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Novel Tunneling Devices for Future CMOS Technologies

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Abstract

Scaling limitations of the conventional MOSFETs demand need for novel ideas and devices. A serious problem with scaling conventional MOSFETs is the enhanced junction tunneling leakage currents due to the non-scalability of the junction electric fields. To overcome this problem, devices based on tunneling currents have been proposed where tunneling currents are no longer an unwanted parasitic effect. The tunnel FET, a three terminal gated p-i-n diode is one such device, originally proposed in III-V compounds and later on silicon. Both lateral as well as vertical structures have been experimentally demonstrated. Even though the devices have very low leakage current, highly suitable for low power applications, the on-current observed is several orders of magnitude less than the industry requirements. Further, detailed study of this device has not been done and it is not understood as to how they behave with scaling. Since the device has different current flow mechanism, it follows different parameter definitions and scaling rules in comparison to the conventional MOSFETs.

In this thesis, using 2-dimensional computer device simulations, a basic understanding of tunnel FETs is developed. A simulation based model is also developed to describe the current-voltage characteristics and to define the electrical parameters of these devices. Since the tunneling currents are weakly dependent on temperature, it is shown that the subthreshold swing is independent of the thermal voltage, kT/q, and hence can be scaled to below this limit. It is further predicted that unlike the conventional MOSFETs, the subthreshold swing is not a constant but is a strong function of the gate bias and can be *vanishingly* small within a small range of gate bias. Thus, it is shown that with proper choice of device geometry parameters, the current can increase several orders of magnitude within a small range of gate bias. Thus, it becomes critical to optimize these devices in the subthreshold region, and gate workfunction is shown to play a critical role.

As low on-currents are observed for silicon tunnel FETs, two optimization schemes are proposed to enhance the tunnel FET on-state performance using SiGe. In the first method pseudomorphically strained SiGe is used to lower the tunnel barrier width to enhance the on-state performance, while in the second method, SiGe is used to lower the tunnel barrier height to enhance the performance. Both the methods have certain advantages as well as disadvantages and a detailed investigation of both the methods is presented. A less than kT/q room temperature subthreshold swing is further predicted.

Experimental verification of the simulation-based model, exponentially increasing transfer characteristics for both the n-channel as well as p-channel operating modes, off-currents less than 100 fA/μm for sub-100 nm channel length devices, and kT/q independent and gate bias dependent subthreshold swing are experimentally verified.

Furthermore, using experimental data, a quality assessment parameter for the tunnel FETs is identified. The forward-biased gated p-i-n diode shows gate induced tunneling currents, resulting in a *peak* in the forward-differential current. The simulations predict that

the peak vanishes for sharper and high source and drain doping profiles, which also result in improved performance for the tunnel FETs.

Due to the extremely low leakage currents, saturation in the output characteristics for sub-100 nm channel length devices, exponentially increasing transfer characteristics for both the sub-threshold as well as the on-region of operation, temperature independent current-voltage characteristics and kT/q independent subthreshold swing, the tunnel FETs look very promising for future scaled CMOS technologies, for both ultra low power and high speed applications.

Keywords: *band-to-band tunneling, gate workfunction engineering, high speed, low-power, novel CMOS devices, surface tunnel transistors, scaling SiGe, simulations, sub-100 nm MOSFET, sub-60 mV/dec swing, subthreshold swing, TFET, tunneling transistor, tunnel FET, vertical MOSFET, Zener tunneling*

Zusammenfassung

Die Grenzen, die der immer weiteren Verkleinerung des konventionellen MOSFETs entgegenstehen, haben es notwendig gemacht, nach neuen Ideen und Bauelementen zu suchen. Eines der Hauptprobleme bei der Skalierung des konventionellen MOSFETs besteht darin, dass sich die elektrischen Felder in den Sperrschichten nicht wie erforderlich verkleinern lassen, was zu erhöhten Tunnelleckströmen in diesen Übergängen führt. Als Lösung dieses Problem wurden in der Vergangenheit Bauelemente vorgeschlagen, die auf Tunnelströmen basieren und in denen diese kein unerwünschter parasitärer Effekt mehr sind. Eines dieser Bauelemente ist der Tunnel-FET, eine mit einem Gate versehene PIN-Diode, der zunächst für III-V-Halbleiter und später auch für Silizium vorgeschlagen wurde. Sowohl laterale als auch vertikale Ausführungen sind bereits experimentel demonstriert worden. Dabei wurde zwar ein, insbesondere für Low-Power-Anwendungen sehr geeigneter, extrem niedriger Leckstrom erreicht, jedoch blieb die Einschaltstromstärke um mehrere Gröβenordnungen hinter den industriellen Anforderungen zurück. Eine detaillierte Untersuchung dieses Bauelements wurde bisher noch nicht durchgeführt, und es ist auch nicht bekannt, wie sich sein Verhalten bei weiterer Skalierung verändert. Da der Stromfluss im Tunneltransistor durch einen völlig anderen Mechanismus gesteuert wird, unterliegt er auch anderen Skalierungsregeln als der konventionelle MOSFET. Diese Arbeit hat das Ziel, mit Hilfe von rechnergestützten, zweidimensionalen Simulationen ein grundlegendes Verständnis des Tunnel-FETs zu entwickeln sowie die Vorteile und Grenzen seiner Realisierung in Silizium aufzuzeigen. Basierend auf Simulationen wird ein Modell entwickelt, mit dem sich die elektrischen Parameter von Tunneltransistoren bestimmen lassen. Außerdem wird gezeigt, dass die Steilheit im Unterschwellenstrombereich nicht wie beim konventionellen MOSFET konstant, sondern eine starke Funktion der Gate-Spannung und zudem unabhängig von kT/q ist, da Tunnelströme nur eine geringe Temperaturabhängigkeit aufweisen. Experimentelle Tunneltransistoren in Silizium bestätigen dieses Modell und zeigen, dass der Einschaltstrom und die Einsatzspannung unabhängig von der Kanallänge sind und dass die Unterschwellstromsteilheit von der Gate-Spannung abhängt. Dies eröffnet die Möglichkeit, die Unterschwellstromsteilheit bei Zimmertemperatur unter die thermische Grenze von 60 mV/Dekade zu drücken, die beim konventionellen MOSFET nicht unterschritten werden kann.

Weiterhin wird ein leistungsfähiger vertikaler Tunnel-FET vorgestellt, bei dem Weite und Höhe der Tunnelbarriere durch eine dünne, dotierte SiGe-Schicht moduliert werden, was zu einer erheblichen Verbesserung des Einschaltstroms, der Einsatzspannung und der Steilheit führt. Zum ersten Mal wird außerdem gezeigt, dass die Steilheit des Tunnel-FET tatsächlich unter die thermische kT/q-Grenze des konventionellen MOSFETs gedrückt werden kann. Ein Ansatz für die Skalierung von Tunnel-FETs wird vorgestellt, der auch bei weiterer Verkleinerung durch Einstellen der Gate-Austrittsarbeit und durch Bandlückenmodulation sehr grosse Ein/Aus-Stromverhältnisse ermöglicht. Da sich mit einer SiGe-Delta-Schicht

allerdings nur die Charakteristik des n-Kanaltransistors und nicht die des p-Kanaltransistors verbessern lässt, wird schliesslich ein leistungsfähiger Tunnel-FET vorgestellt, der das Potential für identische Leistungsdaten sowohl im n-Kanalbetrieb als auch im p-Kanalbetrieb in sich trägt. Möglich wird dies, da der Strom in Tunneltransistoren hauptsächlich durch den Tunnelvorgang dominiert wird und daher unabhängig von der Ladungsträgerbeweglichkeit ist.

Aus den experimentellen Daten ergibt sich ausserdem ein Parameter zur Bewertung der Qualität von Tunneltransistoren. Die in Durchlassrichtung betriebene PIN-Diode mit Gate zeigt einen vom Gate verursachten Tunnelstrom (GIDL), der zu einem lokalen Maximum im um den Bulk-Strom bereinigten Durchlassstrom führt. Aus Simulationen lässt sich vorhersagen, dass dieses Maximum bei höheren Source- und Drain-Dotierungen sowie bei schärferen Dotierprofilen verschwindet, was auch die Tunneltransistorcharakteristik verbessern würde.

Die in dieser Arbeit vorgestellten Tunnel-FETs sind sehr vielversprechend für zukünftige CMOS-Generationen sowohl für High-Speed- als auch für Low-Power-Anwendungen im Analog- und Digital-Bereich.

The principles of physics, as far as I can see, do not speak against the possibility of maneuvering things atom by atom. It is not an attempt to violate any laws; it is something, in principle, that can be done; but in practice, it has not been done because we are too big.

Los Angeles high school could send a pin to the Venice high school on which it says, "How's this?" They get the pin back, and in the dot of the "i" it says, "Not so hot."

-Richard Feynman, *There's Plenty of Room at the Bottom (1959)*

Contents

Nomenclature

α	constant electric field scaling factor
β	inverse thermal factor, q/kT
ϵ_o	dielectric permittivity of air
ϵ_{Si}	dielectric constant of silicon
κ	dielectric constant
λ	channel length modulation factor
μ	carrier mobility
μ_n	electron surface mobility
μ_p	hole surface mobility
ω	tunneling barrier width
ϕ_B	bulk (Fermi) potential
ϕ_S	surface potential
ϕ_{ms}	workfunction difference
ρ	resistivity in Ω-cm
A_{kane}	Kane's first constant
B_{kane}	Kane's second constant
C_D	semiconductor depletion capacitance
C_{ox}	gate-oxide capacitance
E	Electric field in $Volts$/cm
G_{b2b}	band-to-band tunneling generation rate
I	current in $Ampere$
I_{b2b}	band-to-band tunneling current, in $Ampere/\mu$m
I_{bulk}	reverse-biased p-i-n diode current, in $Ampere/\mu$m

I_{DS} drain-source current in $Ampere/\mu$m

I_{off} source-drain off-state current, in $Ampere/\mu$m

I_{VT} I_{DS} at $V_{GS} = V_T$ in $Ampere/\mu$m

k Boltzmann constant 1.38×10^{-23}m^{2}kg-s^{-2}K^{-1}

L device channel length in μm

N_A source doping of a tunnel FET, in cm^{-3}

N_a substrate doping of a conventional MOSFET, in cm^{-3}

n_i intrinsic carrier concentration, in cm^{-3}

q electronic charge, 1.602×10^{-19}C

S subthreshold swing in mV/decade

T temperature, in °C or K

t_{ox} gate-oxide thickness in nm

V voltage in $Volts$

V_T transistor threshold voltage in $Volts$

V_Z p-i-n diode Zener breakdown voltage in $Volts$

V_{DD} Power supply in $Volts$

V_{DS} drain-source voltage in $Volts$

V_{FB} flat-band voltage in $Volts$

V_{GS} gate-source voltage in $Volts$

V_{off} tunnel FET V_{GS} at which I_{b2b} starts to dominate, in $Volts$

W device gate width in μm

W_g energy bandgap, in eV

W_{b2b} band-to-band tunneling width

x Ge mole fraction in SiGe

B^{2}T-MOSFET band-to-band tunneling MOSFET

BJT bipolar junction transistor

CMOS complementary metal-oxide semiconductor

DIBL drain induced barrier lowering

FET field-effect transistor

FIBTET field-induced band-to-band tunneling effect transistor

GIDL gate induced drain leakage

LPCVD low-pressure chemical vapor deposition

MBE molecular beam epitaxy

MOS metal-oxide-semiconductor

MOSFET metal-oxide-semiconductor field-effect transistor

NDR negative differential resistance

PDBFET planar doped barrier field-effect transistor

RIE reactive ion etching

SCE short-channel effect

STT surface tunnel transistor

TBD triangular barrier diode

TEM tunneling electron microscope

TFET tunnel field-effect transistor

VMOS vertical MOS

Chapter 1

Introduction

The advancements in the silicon based complimentary metal-oxide semiconductor (CMOS) technology has led to the phenomenal growth of the semiconductor industry over the last three decades. Scaling of the metal-oxide semiconductor field-effect transistor (MOSFET) is governed by the need for higher speeds and package density (number of components per chip) and low cost per function on the chip. In 1974, Dennard *et al.* [1] proposed scaling criteria for design of MOSFETs at progressively smaller dimensions. In 1975, Moore observed and stated that the transistor performance and density doubles every 2 years [2]. Over the years, the statement became a law, today widely known as the Moore's Law. However, as this scaling of the conventional MOSFETs continue, it is now nearing several theoretical as well as practical limitations beyond which it can no longer be scaled.

In this chapter, a brief discussion of the conventional MOSFETs their scaling limitations and the means by which some of these limitations can be overcome is discussed. A literature review of novel devices recently proposed is then done followed by the scope of the present thesis.

1.1 Conventional MOSFET

The conventional MOSFET is a silicon based device consisting of four regions: the source, drain, channel and a gate (Fig. 1.1). The four electrodes connecting these regions are also named as the source, drain, substrate (connecting the channel with the body of the device) and gate. The gate electrode is separated from the channel by means of an insulating silicon oxide called gate oxide, while the source and drain are separated by the channel which has a charge opposite to that of source and drain. Applied bias at the gate electrode repels the charge in the channel through the *field*[1] in the oxide. At sufficiently large gate bias, a conducting layer is formed close to the oxide-silicon interface, connecting the source and drain regions. This results in the transistor being 'on'. In the absence of the gate bias, no conducting layer is formed and the transistor is 'off' [3]. Thus, the gate controls the transistor turn-on turn-off characteristics. Under ideal conditions, the current flow from the oxide to the gate and in the substrate is zero. Thus, from Kirchoff's law, the current at the source terminal is equal and opposite to that at the drain terminal.

[1] Hence the term 'field-effect'.

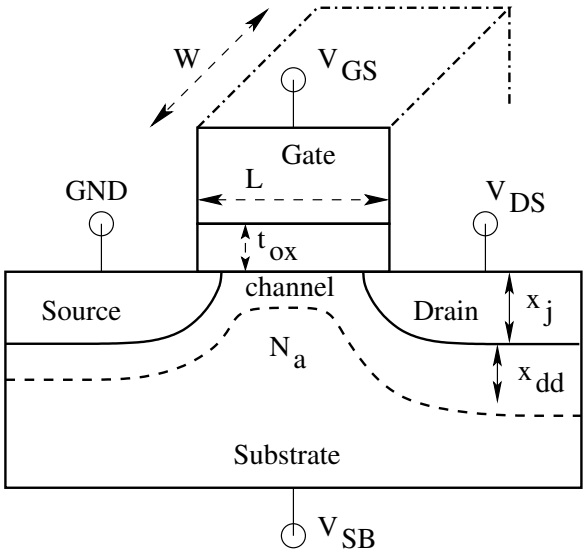

Figure 1.1: *Schematic representation of a conventional MOSFET.*

1.1.1 Device Curves and Equations

[2] Fig. 1.2 shows a typical transfer characteristics (drain current I_{DS} versus gate voltage V_{GS}) of a conventional n-channel MOSFET. There are two regions of operations. The subthreshold region corresponding to the weak inversion of the channel for gate bias, V_{GS}, less than the threshold voltage, V_T; and the on-region, corresponding to strong inversion of the channel for $V_{GS} > V_T$. The drain current, I_{DS}, in the subthreshold region is diffusion dominant and increases exponentially with V_{GS}. In the on-region, I_{DS} is drift dominant and is linear with V_{GS}.

In the absence of the substrate bias, V_{SB}, the surface potential, ϕ_S induced at the silicon (semiconductor)-oxide interface is given by,

$$V_{GS} = V_{FB} + \phi_S + \frac{\sqrt{2qN_a\epsilon_{Si}\epsilon_o\phi_S}}{C_{ox}}. \tag{1.1}$$

V_{FB} is the flat-band voltage or the gate voltage required to produce a zero net electric charge in the semiconductor channel. This is determined by the fixed charge in the oxide (Q_{fc}/C_{ox}) and the workfunction difference, ϕ_{ms}, between the semiconductor and gate electrode material, for example n-type or p-type polycrystalline silicon or metal. At flat-band voltage, the surface potential, ϕ_S is zero and the bands are perpendicular (flat) to the oxide-semiconductor interface. Thus, ϕ_S determines the band bending at the semiconductor-oxide interface resulting from the inversion charge in the channel.

When the surface potential ϕ_S equals twice the bulk (Fermi) potential ϕ_B, which is determined by the doping in the substrate, N_a, and the intrinsic semiconductor carrier concentration, n_i as

$$\phi_B = \frac{kT}{q} ln(\frac{N_a}{n_i}), \tag{1.2}$$

[2]The conventional MOSFET characteristics and parameters are only briefly discussed here. Detailed discussion can be found in standard text books like, S. M. Sze: Physics of Semiconductor Devices [4].

the device is said to be in strong inversion.

Thus, the threshold voltage, V_T corresponding to $\phi_S = 2\phi_B$ at which the transistor starts to conduct is defined as [3],

$$V_T = V_{FB} + 2\phi_B + \frac{1}{C_{ox}}\sqrt{4\phi_B q N_a \epsilon_{Si}\epsilon_o}. \tag{1.3}$$

Here, $kT/q = 25.9$ mV at temperature $T = 300$ K is the thermal voltage (k is the Boltzmann constant and q is the electronic charge). ϵ_{Si} and ϵ_o are the Si dielectric constant and permittivity of air, respectively. C_{ox} is the gate oxide capacitance determined by the gate oxide thickness, t_{ox}.

Thus, the basic equations describing the device characteristics are as follows:

In the subthreshold region,

$$I_{DS} = \mu\frac{W}{L}AC_{ox}e^{\beta\phi_S}(\beta\phi_S)^{-1/2}. \tag{1.4}$$

Here, μ is the carrier (electron or hole) surface mobility (different from bulk mobility), W and L are the device width and channel length, respectively, which define the device lateral dimensions; $\beta = q/kT$ determines the thermal factor at temperature, T. ϕ_S is governed by the channel doping, N_a, ϕ_{ms} and applied gate bias, V_{GS}. For a given device parameters like N_a and drain bias, V_{DS}, A is a constant. Thus, in the subthreshold region, I_{DS} varies exponentially as a function of V_{GS}. The subthreshold swing, S, of the MOSFET, which determines the device turn-off characteristics, is defined as the change in V_{GS} needed to decrease I_{DS} by one decade. From Eq. 1.4, S is given as,

$$S = \frac{kT}{q}ln10.(1 + \frac{C_D}{C_{ox}}) \tag{1.5}$$

where C_D is the depletion capacitance. Thus, for a conventional MOSFET S is independent of V_{DS} and V_{GS} but depends on the substrate doping N_A via C_D, and oxide thickness t_{ox} via C_{ox}. An increase in N_A (lower C_D) and decreasing t_{ox} (higher C_{ox}) result in a stronger gate coupling and hence improved (lower) S. However, S is limited by the thermal factor, β. Thus, at $T = 300$ K, the best achievable value of $S = 60$ mV/decade for $(1 + C_D/C_{ox}) = m = 1$.

In the linear region of operation I_{DS} increases linearly with respect to V_{DS} for a given V_{GS} ($> V_T$).

$$I_{DS} = \mu\frac{W}{L}C_{ox}(V_{GS} - V_T)V_{DS}. \tag{1.6}$$

As V_{DS} further increases, for a long channel length MOSFET, I_{DS} no longer depends on V_{DS} as the depletion width below the drain reduces the channel depth at the drain end to zero. This is the pinch-off point. Thus, in the saturation region of operation, I_{DS} is given by,

$$I_{DS} = \mu\frac{W}{L}C_{ox}(V_{GS} - V_T)^2. \tag{1.7}$$

Fig. 1.3 shows a typical output characteristics (drain current I_{DS} versus drain voltage V_{DS}) of a n-channel conventional MOSFET indicating the various regions of operation as discussed above. For long channel MOSFETs, the source and drain regions are isolated by the channel doping, and the gate essentially determines the potential barrier for charge injection.

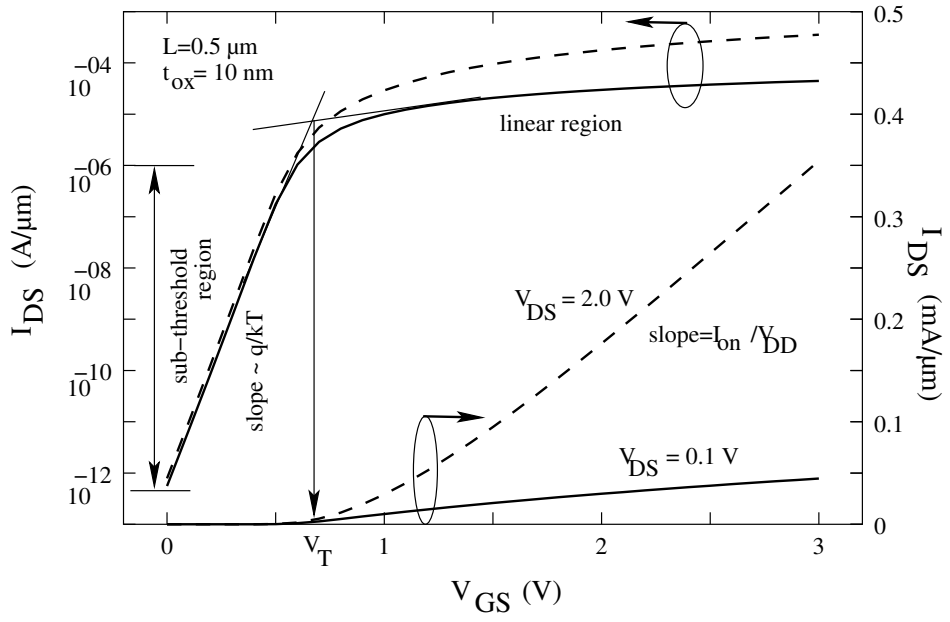

Figure 1.2: *Simulated n-channel transfer characteristics of a long channel conventional MOSFET in the linear as well as the log scale. The MOSFET V_T and subthreshold swing, S are shown.*

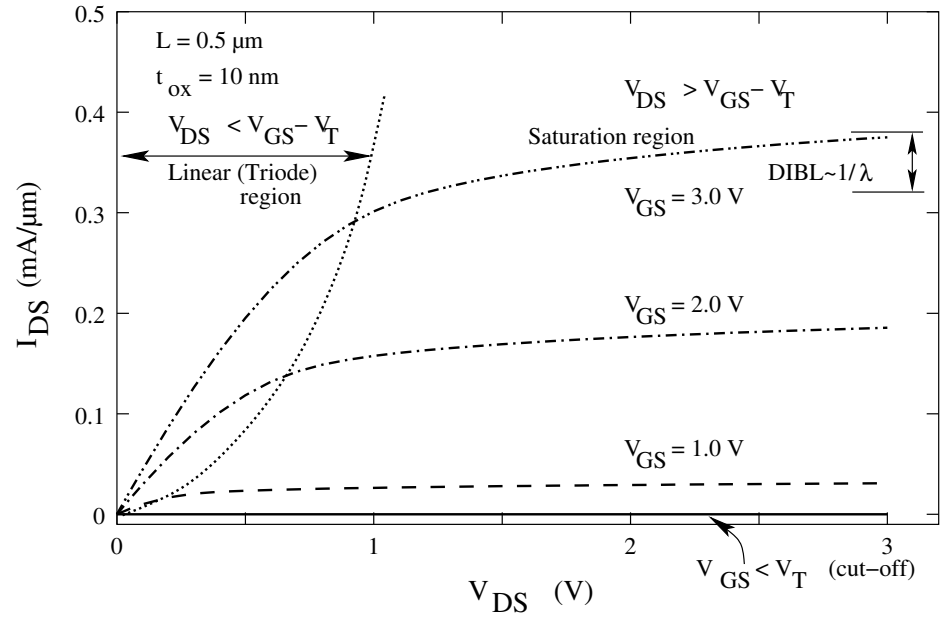

Figure 1.3: *Simulated n-channel output characteristics of a long channel conventional MOSFET. The linear and saturation region of operation are shown.*

The conventional MOSFET is a minority carrier device. The current is determined by the flow of electrons (n-channel) *or* holes (p-channel) across the channel. The p-channel device has doping in the source, drain and channel regions opposite to that of a n-channel device. Since the hole mobility, μ_p is less than the electron mobility, μ_n by a factor of 2 to 3 as a result of their different effective masses, the n-channel and p-channel MOSFETs have *asymmetric* $I-V$ characteristics under similar bias conditions.

1.1.2 Scaling the Conventional MOSFET

In order to improve device performance in terms of speed and device package density on a chip, the most important device parameter to scale is the source to drain distance, or the channel length, L. However, scaling L, leads to several undesirable changes in the device characteristics, jointly termed as the short-channel effects (SCE). These become significant when the depletion region surrounding source and drain extend to large distances in the channel region, and is no longer negligible in comparison to the channel length, L. The gate then starts to lose control over the whole channel. Further, the effective channel length, L_{eff}, determined by the gate controlled part of the channel, and the threshold voltage, V_T of the device change with applied drain bias, V_{DS}. Thereby, leading to drain-induced barrier lowering (DIBL) at the source end and an increase in the off-state current (source-to-drain leakage current).

The scaling rules were first proposed by Dennard *et al.* [1,6] where the authors suggested that the most undesirable short-channel effect was the reduction in the gate threshold-voltage, V_T. They further showed that the short-channel effects can be avoided by scaling down the vertical dimensions (gate oxide thickness, t_{ox}, source/drain junction depth, x_j) along with the horizontal dimensions (L and W) alongside decreasing the supply voltage, V_{DD} and increasing the substrate doping, N_a proportionately. Thereby, maintaining *constant* electric field across the semiconductor junctions and gate oxide. This further leads to an increase in the operating frequency as the circuit delay decreases, and decrease in power dissipation. Thus, for a unitless scaling factor, $\alpha > 1$, the scaling of various device parameters are shown in Table 1.1 [4].

1.1.3 Scaling Limitations of the Conventional MOSFET

Scaling the conventional MOSFET in accordance to the rules stated above have worked well for the last three decades. However, further scaling the device into the sub-100 nm regime faces several theoretical and practical limitations. These arise from fundamental, material, device, circuit and system level scaling [9,10]. Some of the problems related to device scaling, maintaining the constant electric field scaling rules are discussed below.

Power Supply, Threshold Voltage and Subthreshold Swing

As L is scaled down, V_{DD} is reduced as well to keep active power and electric fields within reasonable limits. However, V_T has not scaled as much as the V_{DD} primarily due to its

[3] Note that this is a theoretical definition of V_T for conventional MOSFETs. Experimentally, various other methods have been proposed. This is discussed in detail is chapter 2.

[4] It should be noted that more recently generalized scaling rules have been proposed where the electric field is no longer a constant, see for eg. [7,8].

Table 1.1: *Constant electric field scaling rules [1]*

Scaled Parameters:	
Device dimensions t_{ox}, L, W	$1/\alpha$
Substrate doping, N_a	α
Supply voltage, V_{DD}	$1/\alpha$
Affected Parameters:	
Gate capacitance, C_G	$1/\alpha$
Drain current, I_{DS}	$1/\alpha$
Gate electric field, E	1
Delay time/circuit, $V_{DD}C_G/I_{DS}$	$1/\alpha$
Power dissipation/circuit, $V_{DD}I_{DS}$	$1/\alpha^2$
Power density, $V_{DD}I_{DS}/A$	1

dependence on the off-current, I_{off} (I_{DS} at V_{GS} =0 V, $V_{DS} = V_{DD}$) of the device. It is given by [11],

$$I_{off} = I_{VT}10^{-V_T/S}. \tag{1.8}$$

Since S is largely dependent on the thermally activated diffusion and is independent of L or V_{DD}, scaling V_T would inherently mean trading I_{off}. Also, even if V_T is kept constant, I_{off} would increase in proportion to $1/t_{ox}$ (see Eq. 1.4). Further, CMOS delay increases rapidly when $V_T/V_{DD} > 0.3$ [12]. Since the thermal voltage, kT/q is constant at room temperature, lowering of V_{DD} reduces the ratio between the thermal voltage and V_{DD}. This further leads an increase in the source-to-drain diffusion activated leakage currents [13]. Thereby, putting a limit to scaling V_{DD}. To reduce I_{off} for a scaled V_{DD}, low temperature operating devices are proposed [14–16] which offer improved carrier mobilities and steeper S. Another alternative would be to look for devices with S independent of temperature. Tunneling devices show considerable promise in the later case.

Statistical Fluctuations of Dopant Atoms

Statistical fluctuation of dopant atoms in the channel of MOSFET has been predicted to be a fundamental physical limitation to its scaling [17–20]. There are two aspects of this problem. One is the number of dopant atoms, and the other is their distribution in the channel region. In the sub-100 nm regime, both these lead to non-negligible effects on the device V_T and I_{on} as the number of dopant atoms controlling the device V_T would be less than a hundred. Designing the nanoscale MOSFETs with a thin undoped channel and controlling the V_T by gate workfunction engineering has been suggested as a possible solution [12].

High Field-Effects

High doping pockets in the form of halos at the source/drain ends of the channel have shown to improve the SCE of conventional MOSFET. This, however, creates a high field region near the source/drain regions, thereby leading to large junction leakage currents due to quantum mechanical band-to-band tunneling. This will be discussed in details later in the chapter.

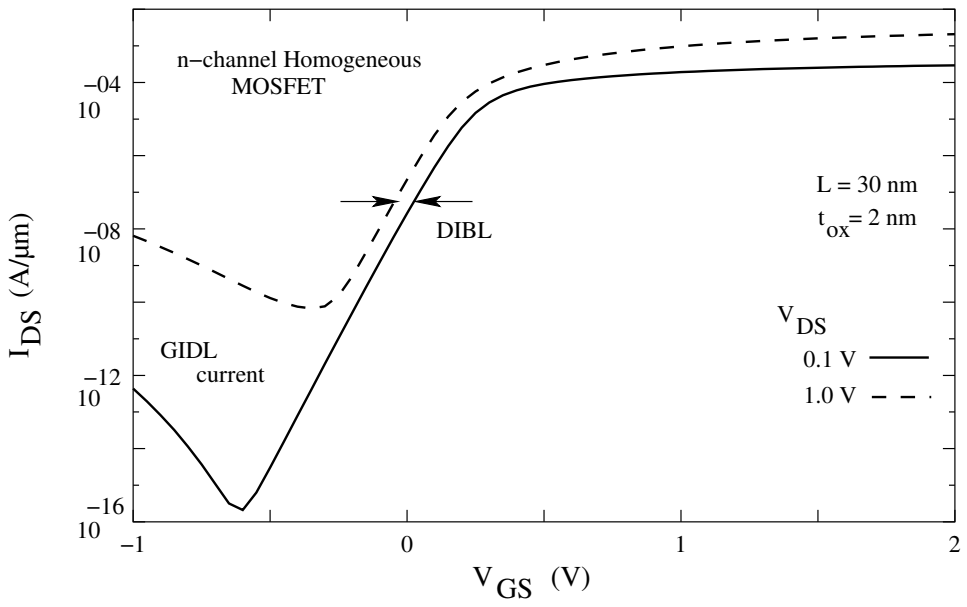

Figure 1.4: *Simulated n-channel transfer characteristics for a short-channel conventional MOSFET ($L = 30$ nm). The change in MOSFET V_T with increase in V_{DS} is shown.*

1.1.4 Short-Channel Effects

Short-channel effects for a conventional MOSFET result when the device channel length is small enough that the drain bias starts to affect the device characteristics. The gate no longer has complete control over the MOSFET turn-on/turn-off characteristics. As a consequence, the output characteristics does not show saturation behavior.

Drain-Induced Barrier Lowering

As L is scaled, for short-channel length devices, I_{DS} is no longer controlled by V_{GS} alone and it starts to increase with increase in V_{DS}. Thus, the output characteristics does not show saturation behavior. The effect is called the drain-induced barrier lowering (DIBL) [5].

$$I_{DS} = \mu \frac{W}{L} C_{ox} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}). \tag{1.9}$$

λ is the channel length modulation factor and depends on L. Fig. 1.4 shows the transfer characteristics for a short-channel length ($L = 30$ nm) vertical MOSFET. Unlike the long channel device (Fig. 1.2), the shift in V_T with respect to V_{DS} is clearly seen. Fig. 1.5 shows the simulated conduction band energy diagrams for a 100 nm channel length conventional MOSFET. The lowering of source-to-drain barrier with increasing V_{DS} lowers the effective channel length of the device. Thus, leading to an increase in current with increase in V_{DS}.

V_T Roll-off

As L is further scaled down, the source-to-drain barrier starts to lower even at $V_{DS} = 0$ V. This leads to a monotonic decrease in V_T with lowering L [21]. This effect is called the V_T roll-off. Fig. 1.6 shows the transfer characteristics for a conventional MOSFET with change

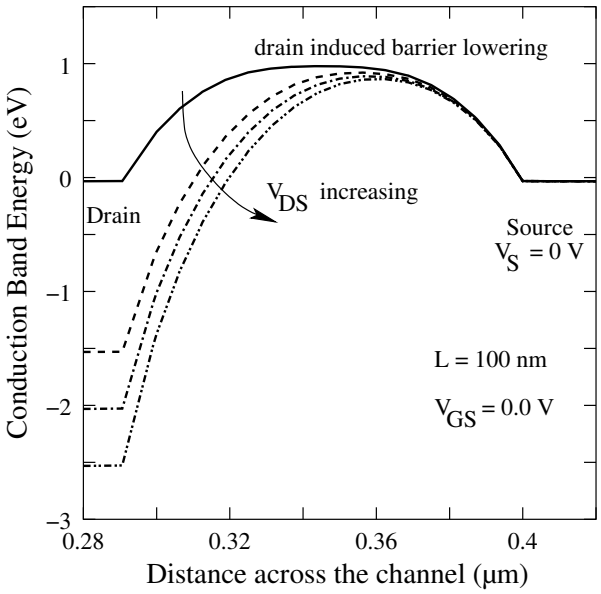

Figure 1.5: *Simulated conduction band energy for a 100 nm conventional MOSFET with change in V_{DS} at $V_{GS} = 0$ V. The lowering of the potential barrier at the source end with increase in V_{DS} is clearly seen.*

in L for $V_{DS} = 0.1$ V. As is seen, even for a fixed V_{DS}, there is lowering of V_T as L is scaled. Fig. 1.7 shows the simulated conduction band energy for change in L at zero bias conditions. The barrier is lowered significantly as L is scaled down.

Halo Engineering

Several optimization schemes have been presented to overcome short-channel effects as the MOSFET is scaled down. Use of halo and non-uniform doping profiles in the channel region have been proposed to overcome SCE by increasing the source-to-drain barrier for current flow [15, 22, 23]. However, it has been shown that they do not fundamentally improve the device performance [24]. The effect of halo doping profile will be discussed in more detail in section 1.2.

1.1.5 Tunneling Leakage Currents

Quantum mechanical tunneling of carriers through the energy barriers in the device is another limiting factor for the scaling of the MOSFETs as they increase the leakage currents significantly. Tunneling from thin gate oxide, band-to-band (Zener) tunneling between the body and drain, and direct source-to-drain tunneling through the channel barrier have been classified as the three major sources of tunneling leakage currents as the devices are scaled down. While the source-to-drain direct tunneling is negligible for $L >$10 nm in silicon [25, 26], the gate oxide tunneling currents are a source of major concern.

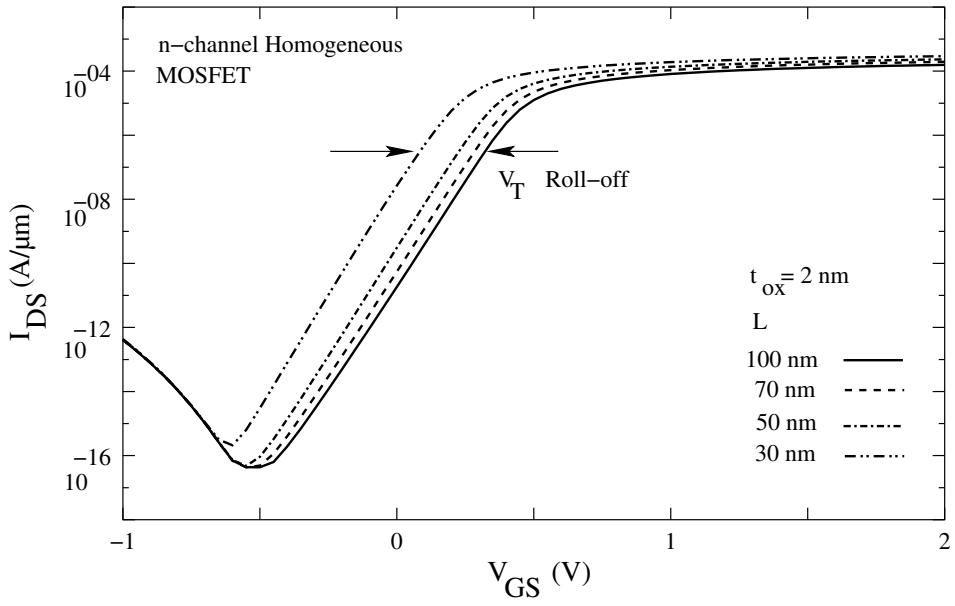

Figure 1.6: *Simulated n-channel transfer characteristics for conventional MOSFET for L changing from 100 nm to 30 nm at $V_{DS} = 0.1$ V at constant $t_{ox} = 2$ nm. V_T is lowered as the potential barrier is lowered with L scaling.*

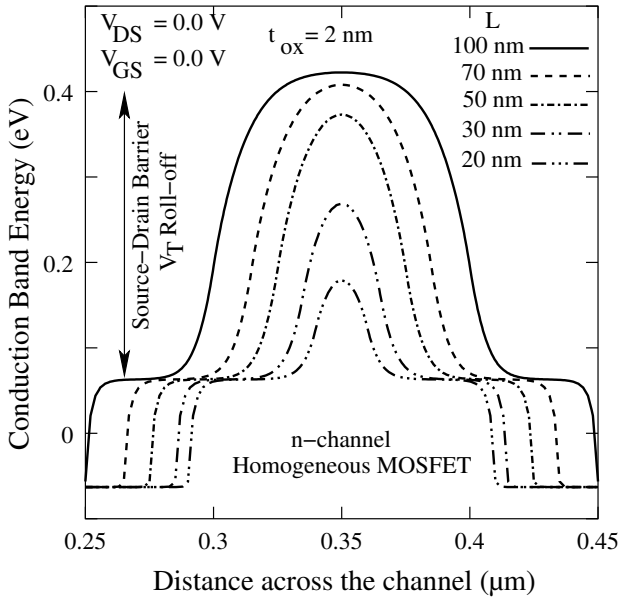

Figure 1.7: *Simulated conduction band energy for a n-channel conventional MOSFET for change in L from 100 nm to 20 nm at $V_{GS} = 0$ V $= V_{DS}$.*

Gate Oxide Leakage Current

As indicated in Table 1.1, to avoid SCE and maintain constant electric field in the oxide, the gate oxide thickness, t_{ox}, is scaled in proportion to L and W. However, as t_{ox} is scaled, tunneling leakage currents through the oxide start to increase [27, 28]. Lo *et al.* [29] showed that the silicon oxide can be thinned down to slightly below 2 nm before the leakage currents are large enough to be unacceptable. Since the tunneling takes place not only in the inversion layer, but also in the accumulation region where the gate overlaps the source and drain, this later component too becomes significant as the devices are scaled down [30]. Using physically thicker gate insulating material with dielectric constant, κ, higher than that of silicon-oxide has been suggested as a possible solution to reduce the direct tunneling through the insulator [31, 32]. However, the thickness cannot grow unlimited as 2-D effects in the thicker insulator start to interfere with scaling [33]. The short-channel performance is degraded due to the fringing fields from the source/drain regions which become non-negligible as the thickness-to-length aspect ratio increases [34, 35].

Gate Induced Drain Leakage Current

As the conventional MOSFET gate oxide thickness is scaled, the fields in both the oxide and silicon in the gate-drain overlap region increase. The large fields deplete the drain overlap region leading to significant band bending. This leads to a band-to-band tunneling current in the gate-overlap, deep-depleted drain regions. This Gate Induced Drain Leakage (GIDL) current has been well observed in conventional MOSFETs and seen to degrade the short-channel performance and leakage currents [36–40]. The GIDL current shows a strong gate and drain bias dependence. As the MOSFETs channel length is scaled, the non-scalability of the overlap region results in an enhanced degradation of the device. The GIDL current, however, is strongly dependent on the drain doping profile. For low drain doping, even though the band bending is significant, the depletion width is too wide to cause significant tunneling current. Similarly, for very high drain doping, even though the depletion width is very narrow, the Fermi potential gets pinned which prevents band bending at the oxide-silicon interface and hence suppresses the tunneling leakage currents. Thus, the GIDL currents exist only within a certain doping range.

1.2 Vertical Field-Effect Transistor

Vertical, or v-groove MOSFETs (Fig. 1.8) have both technological as well as device level advantages over conventional lateral MOSFETs [41]. Since L is determined by epitaxy and not by photolithography it can be scaled to any desired channel length. Gate all-around structures account for high current drive by increasing the effective channel width by a factor of four as compared to the lateral structures. Thus, increasing the package density considerably. Further, thin and fully depleted pillars provide better control over the substrate depletion region and hence improve short-channel performance. Very short-channel length vertical MOSFETs have been demonstrated with drain current and transconductance values comparable to very advanced planar MOSFETs [42].

However, the vertical structures have several disadvantages because of which they have not yet been adpoted in mainstream research. One of them is the large gate overlap capacitance as a result of surrounding gate. Further, no promising solution exists in literature

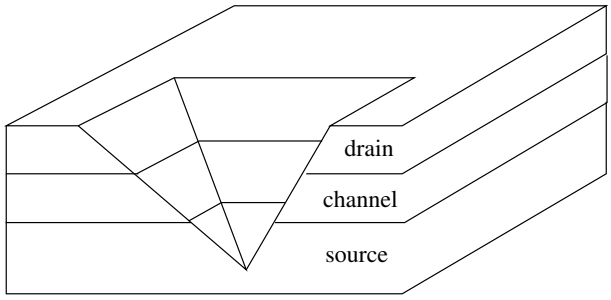

Figure 1.8: *Schematic representation of the vertical MOSFET structure layers. The gate is vertical on the sidewalls on all four sides. The earlier vertical structures were etched isotropically, reasulting in a 'v' structure as shown here.*

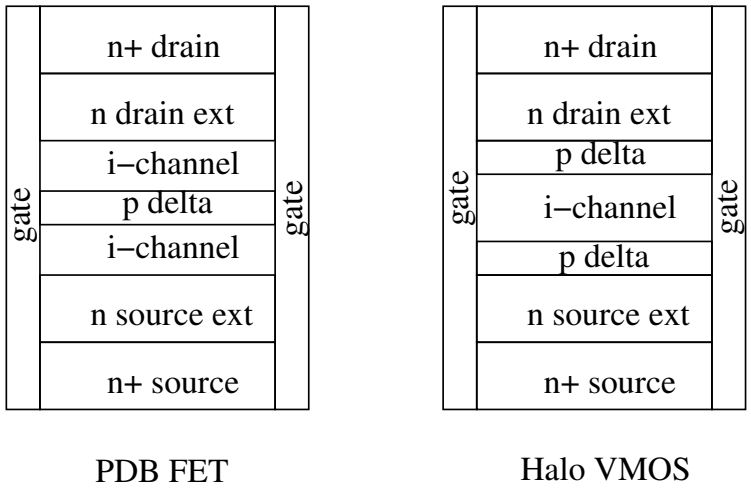

Figure 1.9: *Schematic representation of the vertical n-channel MOS structures: PDBFET and halo-VMOS. Anisotropic etching by reactive-ion etching (RIE) result in vertical structures.*

for realization of vertical 3-D circuits. Recently, vertical structures have been proposed for improved performance in terms of drive current, transconductance and reduction of large gate overlap capacitance associated with vertical structures [43, 44].

Precise control of dopant atoms during epitaxy growth leads to the possibility of achieving very sharp and abrupt doping profiles [45]. The planar-doped-barrier (PDB) FET has also been demonstrated to further the scaling of vertical MOSFETs with improved performance [46–49]. The device consists of a thin delta doped layer sandwiched in the middle of the intrinsic channel (Fig. 1.9). This leads to a triangular potential barrier between the source and drain, the height of which is determined by the delta doping. Unlike the conventional long channel MOSFET, where the potential is uniform across channel and the maximum value of the lateral electric field appears at the source end, for the PDBFET, the peak electric field is determined by the position of the delta layer [50, 51]. While shifting the delta layer towards the source end can significantly improve the device punch-through effect [52], optimum performance is achieved by having it in the middle of the channel [53].

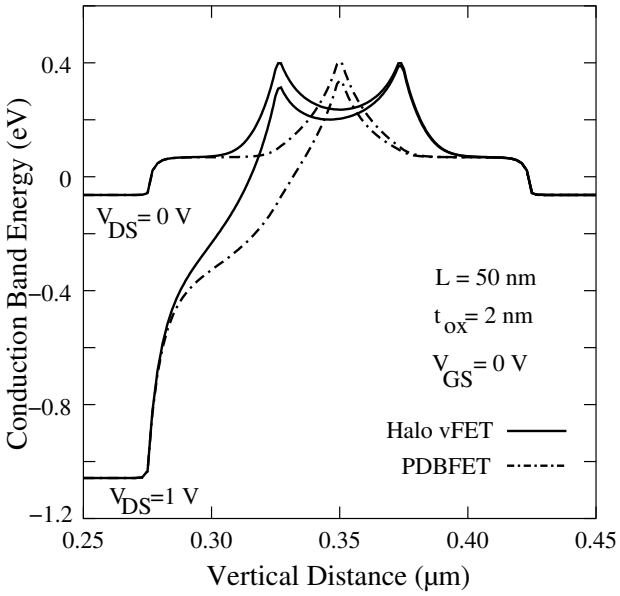

Figure 1.10: *Conduction band diagrams for a PDBFET and a halo VMOS. The halo device is much more robust to the SCE in comparison to the conventional VMOS and the PDBFET.*

Since the diffusion barrier is essentially controlled by the doping in the delta layer, the V_T and L_{eff} of the PDBFETs is determined by the delta layer doping and thickness. As the PDBFET is scaled, the drain bias start to lower the barrier resulting in SCE [50]. An increase in the delta doping results in an improved SCE trading-off V_T which also increases. A halo vertical structure where the VMOS characteristics is determined by *two* delta doped layers, one at the source and drain end each (Fig. 1.9), provides a solution to improve the SCE in VMOS structures, similar to that of the conventional *halo* MOSFETs. Fig. 1.10 shows the conduction band diagrams for a 100 nm n-channel PDBFET and a halo VMOS structure for constant doping in the delta layer of the PDBFET and that of the halo FET ($1.5\times10^{19}\text{cm}^{-3}$). The dopings in the delta layers are so chosen to have the same V_T for both the device structures. While the drain bias lowers the barrier for the PDBFET resulting in DIBL; for the halo VMOS, even though the drain end barrier is lowered, the barrier at the source end is unaffected resulting in improved SCE. Fig. 1.11 shows the simulated transfer characteristics for the halo VMOS and the PDBFET for L varing from 100 nm to 20 nm. Improved SCE in terms of V_T rolloff, leakage currents and DIBL are observed. However, having a delta layer each at the source and drain end result in large electric fields across the source and drain junctions. Thus it becomes necessary to incorporate the lightly-doped source and drain regions. Further optimization of the devices has been proposed by means of asymmetric channel doping profiles.

1.3 Novel Devices

Several novel device architectural concepts have been proposed to overcome the shortcomings of the scaled conventional MOSFET. One of the fundamental limitations of conventional MOSFET is the non-scalability of room temperature S, which limits the I_{on}/I_{off} ratio.

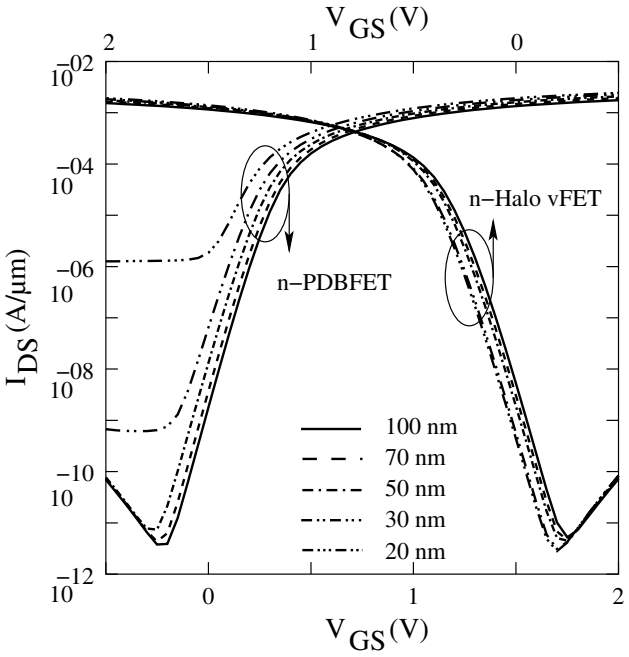

Figure 1.11: *Input characteristics of a halo VMOS and a PDBFET for L varying from 100 nm to 20 nm, shows the improved SCE for the halo FET in comparison to the PDBFET.*

Advanced 3-dimensional architecture like the Fin-FETs with very thin mesas and multiple gates [54, 55], and, silicon-on-nothing [56] structures have been proposed. Thus a strong gate coupling result in close to the ideal room temperature S values.

Devices based on gate controlled impact-ionization in silicon have been shown to have very large turn-on turn-off behavior independent of kT/q in vertical PDBFETs [57] and gated p-i-n diodes [58, 59]. Such devices, though are associated with reliability problems, and are not temperature independent [60]. However, large hysteresis behavior is observed at room temperature in PDBFETs [57] which further degrade at lower temperatures [61]. Further, in the p-i-n diodes, hot carrier effects lead to a degradation in the device V_T and S with stress cycles [62, 63].

1.3.1 Tunneling Devices

Devices based on tunneling currents have also been proposed, where the device on-current is determined by gate controlled tunneling. Since the probability of tunneling depends on tunneling barrier height and width, and is nearly temperature independent, these devices show a nearly temperature independent $I - V$ characteristics which allow reliable operation of such devices at both low and high temperatures. Further, tunneling currents are no longer an unwanted parasitic effect in these devices. Thus, three terminal band-to-band tunneling transistors (B^2T-MOSFET) based on gate induced drain leakage (GIDL) current resulting from tunneling in gate-source overlap regions [64, 65], and tunneling from Schottky barriers have been proposed [66, 67]. While the former failed to meet the International Technology Roadmap for Semiconductor (ITRS) [68] requirements in term of I_{on}, the later has high leakage currents.

In order to overcome problems like the statistical distribution of dopant atoms in the channel and high electric field induced tunneling leakage currents in conventional MOSFET, room temperature transistor behavior in three terminal gated p-i-n diodes [69] was first proposed in III-V compounds [70, 71] and later in bulk silicon [72, 73] and more recently in gated p-n junctions in silicon-on-insulator [74]. Gate controlled negative differential resistance (NDR) was further observed in these devices based on forward biased Esaki [75] tunneling [76–79]. Field-induced band-to-band tunneling effect transistor (FIBTET), with degenerate source, drain and channel regions have also been demonstrated which show NDR behavior [80]. Multiple resonant peaks have also been demonstrated in similar device structures [81].

We have demonstrated similar tunnel FET behavior in molecular beam epitaxy (MBE) grown vertical gated p-i-n diodes on silicon as a possible candidate for future CMOS technologies [82–85].

1.4 Scope of the Present Work

The proposed tunnel FETs, as discussed in the earlier section, show a lot of promise for future CMOS technologies as a alternative to the conventional MOSFET. However, a thorough study of these devices have not yet been done. Further, low on-current is observed in these devices, and no conclusive solution has been provided for the same.

In this thesis, using 2-dimensional computer device simulations, a basic understanding of the tunneling FETs is developed and presented. The simulation model used for the purpose is discussed in detail and experimental justification of the same is provided. Using the model, it is predicted that with δp^+ SiGe layer at the p^+source end, the n-channel tunnel FET performance can be significantly improved in terms of I_{on}, V_T and S, to meet the technology requirements. It is further shown, for the first time, that the swing of tunnel FETs is not a constant, but is strongly V_{GS} dependent. Below V_T, I_{DS} is falling *faster* than exponential. This allows the possibility of optimizing the tunnel FET effective room temperature subthreshold swing (average swing below V_T) to be *less* than the conventional MOSFET thermal limit of 60 mV/dec. Thus, the tunnel FETs can be scaled maintaining large I_{on}/I_{off} ratios.

Since the tunnel FET has different current flow mechanism (tunneling currents for both the subthreshold region as well as the on-region of operation), as compared to the conventional MOSFETs where the current is due to diffusion (subthreshold region of operation) and drift-diffusion (on region of operation), the tunnel FETs follow different scaling rules and parameter definitions.

Further, as the tunnel FET current flow for both the n-channel as well as p-channel operation mode is due to electrons tunneling from the valence band to the conduction band, the devices can be realized with symmetric performance. This is unlike the conventional MOSFETs where the difference in electron and hole mobilities force the requirement of different channel width for n-channel and p-channel FETs. Thus, finally, a high performance lateral symmetric tunnel FET for both high speed and low operating-power applications for future CMOS technologies is demonstrated.

Chapter 2

Tunnel Field-Effect Transistor

Tunnel transistors have several immediate advantages over conventional MOSFETs. Since tunneling takes place in a very small region, the gate length of these device can be scaled to the distance of the tunneling barrier width which is less than 10 nm in silicon. As the source-to-drain direct tunneling can be neglected for channel length greater than 10 nm in silicon, tunnel FETs can be scaled to the ultra short-channel region without significant loss in the off-currents. As the device parameters are independent of channel length, statistical variations in threshold voltage, off- and on-current, due to the mask level variation in channel length is absent.

Tunnel currents are only indirectly and weakly dependent on temperature. Tunneling devices, thus, show a very weak temperature dependence, and allow reliable operation at both low as well as high temperatures. The current-voltage characteristics is further independent of the kT/q thermal factor, which allows the possibility of optimizing them with a sub-60 mV/dec subthreshold swing at room temperature. Thus, overcoming the thermal limit of the conventional MOSFETs.

As the conventional MOSFETs are scaled into the ultra short channel region, tunneling from heavily doped junctions result in large parasitic leakage currents. Since the on-current of tunnel transistors is determined by tunneling, this is no longer an unwanted parasitic effect. Furthermore, the current is exponentially increasing for both the on-region as well as the off-region of operation. This puts them at par with the bipolar-junction transistors (BJTs). The collector current, I_C, of the BJT varies exponentially with the base-emitter voltage, V_{BE} as

$$I_C = I_s exp \frac{qV_{BE}}{kT} \tag{2.1}$$

where I_s is the saturation current at constant collector-emitter voltage V_{CE}.

Gate controlled band-to-band tunneling in three terminal gated p-i-n diodes have been demonstrated in both lateral as well as vertical MOSFETs. Tunnel transistors based on band-to-band tunneling (B^2T-MOSFET) from the deep-depletion region in the gate-source overlap region have been demonstrated [64, 65]. The first gated p-i-n diodes operating as Surface Tunnel Transistors (STT) were proposed on III-V compounds [70,71]. The tunneling current results from interband tunneling from a degenerate p^+drain to a two dimensional electron gas (2DEG) in the channel, which resulted from an applied gate bias. The depth of

the inversion channel determins the cross-section area of the tunneling p-n junction, while the electric field at the tunnel junction is essentially controlled by the gate bias.

Similar lateral interband tunneling transistor operation was then demonstrated in silicon [72, 73]. Room temperature gate controlled negative differential conductance based on Esaki tunneling was further observed in these devices [76–79]. Esaki tunnel transistors were then demonstrated in vertical gated p-i-n diodes [82–85] and very recently also in lateral gated p-n junction diode on silicon-on-insulator (SOI) [74]. While the absence of channel length in the gated p-n diode (termed as lateral interband tunneling transistor or LITT) resulted in improved gate capacitance; it did not fundamentally improve the on-current, which was still several orders of magnitude less than the technology requirements. Further, it also resulted in large junction fields at zero gate bias condition. Thereby, leading to an increase in leakage currents.

A p-i-n diode configuration for the tunnel FETs provide a large source-to-drain diffusion barrier, as compared to the n-p-n configuration of the conventional MOSFETs. This results in several orders of magnitude lower diffusion leakage currents in tunnel FETs, making them ideal for low power applications. Further, the 'i' region is ideally intrinsic and the threshold voltage of the tunnel FETs is determined by the band bending (tunneling width) at the tunnel junction. This avoids the problems related to the statistical fluctuation of dopant atoms in the channel even as the devices are scaled down.

However, due to smeared-out doping profiles at the tunnel junction, and large indirect bandgap of silicon, these devices show a large threshold voltage, V_T, resulting in a very low on-curent, I_{on}, at reasonalble supply voltages. Even the first epitaxially grown vertical tunnel FETs showed poor saturation behavior in the output characteristics, large leakage current, I_{off}, and very low on-current of the order of 10 nA/μm [84].

Thus, even though various tunnel FET structures have been recently demonstrated as possible candidates for future technologies as an alternative to the conventional MOSFET, a thorough study of these devices has not yet been done. Further, the high V_T and low on-current of tunnel FETs is still a problem and no conclusive solution has been provided for the same. It has also not been realized as to how these devices behave at scaled dimensions in comparison to the requirements of future CMOS technology. Since the tunnel FETs have different current-voltage mechanism, they are expected to follow different scaling rules and electrical parameter definitions as compared to the conventional MOSFETs.

In this chapter, a simulation based study is done to develop a basic understanding of the tunnel FETs. This helps in determining the various device and geometry parameters that essentially control the tunnel FET electrical parameters. This is also essential for further optimization of the device. A detailed discussion is done on the simulation tools and interband tunneling model used for the purpose. The validity of the tunneling model is confirmed by showing that the simulation results give a good match with the earlier experimentally demonstrated tunnel FET on silicon [86]. Since the tunnel FETs have different current flow mechanism in comparison to the conventional MOSFETs, it is shown that the device characteristics can be described by one equation for both the on-state as well as the off-state of operation. Thus, the electrical parameters, V_T and swing, S, for tunnel FETs which show different behavior, are defined. It is further shown, that unlike the conventional MOSFETs, S is not a constant in the subthreshold region, but is a strong function of gate bias.

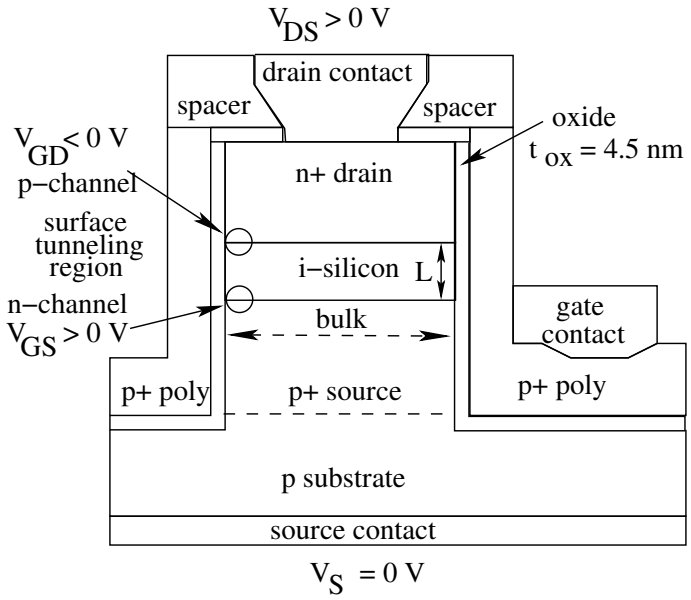

Figure 2.1: *Schematic representation of a vertical tunnel FET structure. The surface tunneling region for both the n-channel as well as the p-channel operating mode is shown. The thickness of the i-Si layer determines the channel length, L, while the mesa width determines the device width, W.*

2.1 Device Structure

The tunnel FETs demonstrated in direct bandgap materials [71] have few orders of magnitude higher on-current as compared to the silicon tunnel FETs. Thus, in order to achieve similar performance for the silicon tunnel FETs, even under optimum geometry parameters, an extremely high and abrupt doping profile is needed. Epitaxy by molecular beam epitaxy (MBE) or low-pressure chemical vapor depostion (LPCVD) allows growth of such devices at temperatures below 750°C. Thus, a vertical structure is chosen for our purpose outlined in the previous section. It should be noted, that apart from the device geometry, the basic device working principle is the same. Thus, the discussion applies equally well to both the lateral as well as the vertical structures.

The device structure is very similar to our earlier demonstrated epitaxially grown tunnel FETs [82, 83, 85]. While the earlier devices were grown on a n^+ substrate with p^+ drain on top, for all the discussion in this thesis, the device grown on a p^+ substrate with an n^+ drain on top [86] is chosen. Thus, the source (connecting the p^+ region via the substrate), the drain (connecting the n^+ region), and a vertical gate which is separated from the other regions via an insulating oxide material, form the three terminals of the device. The thickness of the 'i' region determines the channel length, L, of the tunnel FET, while the mesa width determines the channel width. Fig. 2.1 shows the schematic representation of the device. The various layers were grown on a p^+ boron doped <111> substrate ($\rho < 0.02$ Ω-cm) which also acts as the source electrode. In order to obtain a high and a sharp doping profile, a 3 nm highly doped boron delta-layer (δp^+) was deposited on top of the substrate. This was followed by a 100 nm lightly doped 1×10^{16} cm^{-3} n^- region which determines the channel, and a 300 nm 1×10^{20} cm^{-3} n^+ doped top drain electrode. Thus forming a p-i-n diode. The n^- doping in

the channel region arises due to the unintentional doping during MBE growth[1]. After mesa etching, a nominally 16 nm thick silicon oxide was thermally grown by annealing in oxygen ambient at 800°C for 30 minutes. 300 nm of n^+ polysilicon was deposited to form the gate electrode. The gates were patterned and isolated with an LPCVD nitride. Contact vias were etched in the nitride and Al was then deposited to form the top drain contact. Metallization of the back side of the wafer was done to form the back source contact. All the process steps were optimized so that the temperature does not exceed 800°C. This is essential to prevent the out-diffusion of boron. The fabrication method of this device has been discussed in detail in [86].

2.2 Working Principle

The surface tunnel transistor works as a gate controlled transistor when the p-i-n diode is reverse-biased. The gate controls the surface band-to-band tunneling width and hence the tunneling current. In the absence of gate bias, V_{GS}, the tunneling probability is low and only reverse-biased bulk p-i-n diode leakage current, I_{bulk}, is observed. I_{bulk} is diffusion dominant and is of the order of 1 fA/μm for a 100 nm intrinsic region[2]. Thus, for $V_{DS} < V_Z$, where V_Z is the reverse-biased p-i-n diode Zener breakdown voltage, I_{bulk} depends on the device geometry parameters L and W, dopings in the three regions, the crystal quality, and the sharpness of the doping profile. It is however, nearly independent of t_{ox} and the gate bias, V_{GS}. Thus, when the band-to-band tunneling probability is low at $V_{GS} = 0$ V, I_{bulk} determines the leakage current of the tunnel FET, I_{off}. Since the p-i-n diode configuration results in a full thermal diffusion barrier for electrons and holes, as compared to only half for the conventional MOSFETs, I_{off} is ideally very low.

Application of a positive gate potential ($V_{GS} > 0$) accumulates the n^- channel. This creates a sharp p^+n^+ tunneling junction between the source and the channel. The gate controls the electron concentration in the channel, and hence the p^+n^+ tunneling junction width for electrons tunneling from the valence band in the p^+source to the conduction band in the channel. At sufficiently high $V_{GS} = V_{off}$, when the tunneling probability is significant, the band-to-band tunneling current, I_{b2b}, becomes more dominant than the constant I_{bulk}. Beyond this point, the tunnel FET drain current, I_{DS} which is defined as,

$$I_{DS} = I_{bulk} + I_{b2b} \tag{2.2}$$

starts to increase exponentially with increase in V_{GS}. This is because I_{b2b} increases exponentially with increase in V_{GS}. Thus, the application of a positive gate voltage leads to a lowering of tunneling barrier width resulting in a tunneling current from p-source to the n-drain. This is defined as the n-channel operating mode of the device.

Similarly, when a negative potential ($V_{GS} < 0$) is applied to the gate electrode, a hole inversion channel is formed. This results in a n^+p^+ tunneling junction between the n-drain

[1]It should be noted, that the unintentional low doping in the i-region is due to the technological limitations and both n-type or p-type doping profile is possible. Since this does not affect the tunnel FET performance as such, the choice of an n^- doping for the 'i-Si' is done for all the simulations results presented in this work. This corresponds to the doping level of our MBE system.

[2]Ideally, for a sharp and abrupt doping profile of the p-i-n diode, I_{bulk} is independent of the i-silicon thickness. However, due to smear-out of the doping profile, the effective fields are determined by the sharpness, and doping level of the p-n junction thus formed.

and the channel. This is defined as the p-channel operating mode of the device where the electrons tunnel from the valence band in the channel to the conduction band in the n^+ drain.

Unlike the conventional MOSFET, where the terms n-channel and p-channel imply the *electron*-induced or the *hole*-induced current flow; for a tunnel FET, the terms are used to distinguish whether the tunneling junction is created by electrons (n-channel) or by holes (p-channel) in the intrinsic silicon region. The current flow, though, for *both* n-channel or p-channel device is due to *electrons* tunneling from the valence band to the conduction band. Thus, with a mid-bandgap gate material, intrinsic channel and symmetric n^+ and p^+ drain and source doping profiles, the tunnel FET on silicon has symmetric n-channel and p-channel current-voltage characteristics. This, again is an advantage over the conventional MOSFETs where the current-voltage characteristics are not symmetric due to the difference in electron and hole mobilities. Thus, while the channel width, W, for a given technology node for conventional MOSFETs is different for n-channel and p-channel devices, for the tunnel FET, the same width is needed.

When the p-i-n diode is forward biased, the device shows forward-biased p-i-n diode characteristics for zero gate bias. Gate controlled NDR has also been observed in forward-biased surface tunnel transistors with heavily doped source and drain regions [76, 77].

Thus, while the drain bias switches the device characteristics from that of a forward-biased p-i-n diode to that of a tunnel transistor; the gate bias switches the tunnel transistor characteristics from a n-channel to a p-channel transistor, when the diode is reverse-biased.

2.2.1 Band Diagrams and Tunneling Widths

Figures 2.2 and 2.3 show the simulated band diagrams for the n-channel tunnel FET as a function of gate-bais and drain-bias, respectively. The cutline is taken close to and parallel to the Si-SiO_2 interface (ref. Fig. 2.1). The parameters chosen are the same as for the experimentally fabricated device as described above. When a positive gate potential, V_{GS}, is applied, it causes accumulation of electrons in the channel. The highly doped δp^+ layer at the p-source end, causes a pinning of the Fermi level with respect to both V_{GS} and V_{DS}. However, in the channel region, there is significant band bending due to the gate potential (Fig.2.2). This results in lowering of the tunneling barrier width, ω, at the source end.

On application of a small positive drain potential, V_{DS}, (reverse-biasing the p-i-n diode), the bands are pulled down at the n-drain end (Fig. 2.3). Thereby, further lowering ω at the p-source end. This will in turn result in an exponentially increasing drain current. However, increasing V_{DS} further leads to the saturation of ω and the drain current shows quasi-saturation. At sufficiently high V_{GS}, the electric fields in the tunneling region are determined by the gate-bias, and the device performance is essentially independent of V_{DS}. Thus, under ideal conditions, the tunnel FETs show excellent saturation behavior.

2.3 2-Dimensional Tunnel FET Simulation Tools and Models

In order to have a better understanding of the devices, and to compare them with the technology requirements and for future optimization, it often becomes necessary to study them under ideal conditions. 2-dimensional (2-D) computer device simulations therefore provide a useful tool for such purposes. Further, it also provides an easy and cost-effective

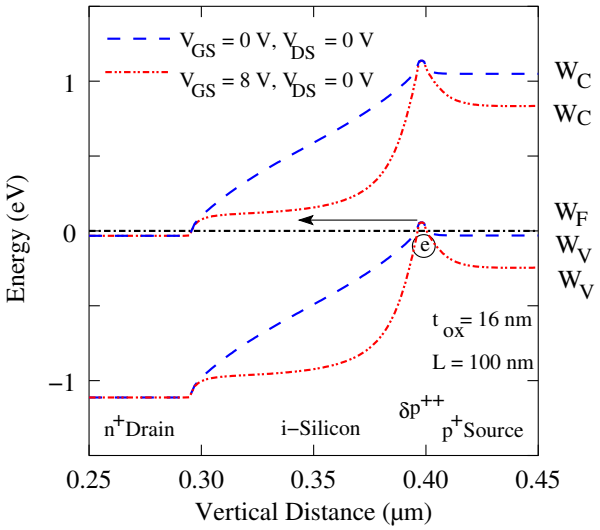

Figure 2.2: *Band diagram for vertical tunnel FET for change in gate bias, V_{GS}. ω is lowered significantly with increase in V_{GS}.*

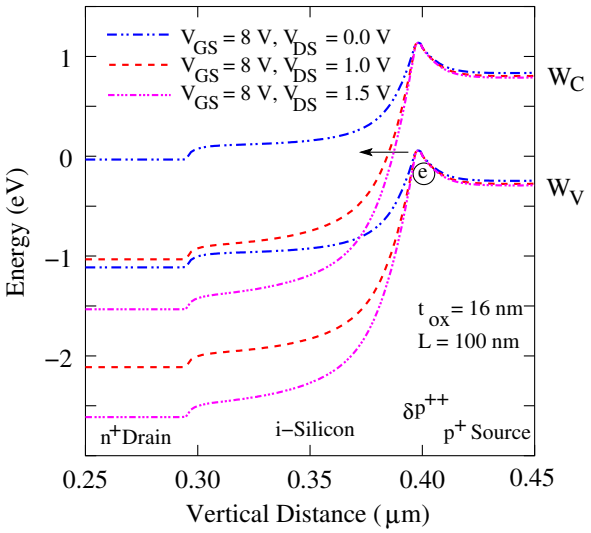

Figure 2.3: *Band diagram for vertical tunnel FET for change in drain bias, V_{DS}. ω is initially lowered and then reaches saturation.*

way to understand the performance of the device, both qualitatively and quantitatively, with change in parameters like doping concentrations, t_{ox}, and L. Taking the experimental device as reference, optimization becomes fast.

In the following sub-sections, a brief discussion of the theory of tunneling is done followed by the applicability of the band-to-band tunneling model available in a commercially available 2-D device simulator, MEDICI [90], for the tunnel FET.

2.3.1 Theory

Electrical breakdown of solids was first observed by Zener [91]. Esaki [75] discovered that p-n junctions in germanium made from material doped to degeneracy have a current-voltage characteristics with an *anomalous* negative-conductance region in the forward direction. This phenomena, he believed represented majority carrier tunneling between the bands inside the tunneling region. Fig. 2.4 shows the schematic representation of the silicon band structure. Silicon is an indirect bandgap material. That is, the minimum of the conduction band does not lie at the same place as the maximum of the valence band in the momentum (k) space. Thus, tunneling in silicon would involve both a change in energy as well as momentum. If the momentum difference between the tunneling states is supplied by a scatterer such as phonon or impurities, tunneling can take place. Theory of tunneling in both direct bandgap materials [92] and well as indirect materials [93–96] has been studied extensively.

MEDICI uses the Kane's model [92] to model band-to-band tunneling in silicon. Even though the Kane's model has been derived for tunneling in direct bandgap materials, it has been shown to give a good match for band-to-band tunneling in Si tunnel FETs at both high temperatures as well as low temperatures [97]. In the following, good agreement of the same is also shown with our experimentally demonstrated Si tunnel FET [86]. A simple simulation based approach is adopted, by first solving the Poisson's equations for the 2-D

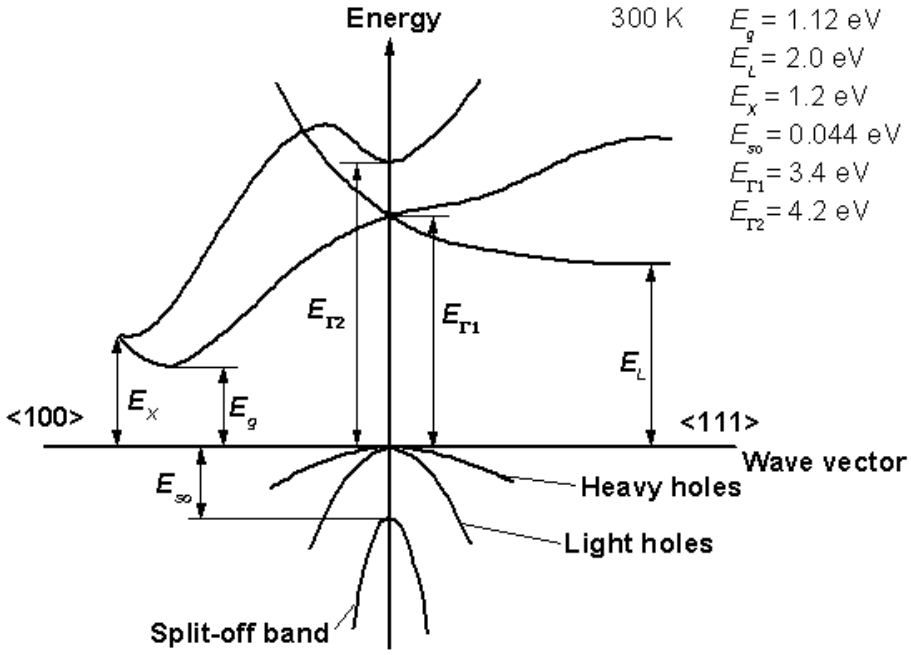

Figure 2.4: *Schematic representation of the silicon band structure. Vertical axis is energy while horizontal is electron or hole momentum in <111> or in <100> k-space directions.*

device geometry to calculate the maximum electric field across the tunneling junction. It is then show that the afore-mentioned field-dependent Kane's model gives a good match with our experimentally demonstrated tunnel FET on silicon.

2.3.2 Kane's Interband Tunneling Model

Field-dependent band-to-band tunneling generation rate, G_{b2b}, as given by the Kane's model is,

$$G_{b2b} = A_{kane} W_g^{-1/2} E^2 exp(-B_{kane} W_g^{3/2}/E). \tag{2.3}$$

E is the electric field across the tunneling junction and W_g is the bandgap. The two constants,

$$A_{kane} = \frac{e^2 m_o^{1/2}}{18\pi\hbar^2} \tag{2.4}$$

and

$$B_{kane} = \frac{\pi m_o^{1/2}}{2e\hbar} \tag{2.5}$$

are Kane's first and second constants, respectively. Both, A_{kane} and B_{kane}, in general, are functions of carrier effective mass, m_o, but are assumed to be constants in MEDICI; for example, they do not vary with applied voltage. e is the electronic charge and $\hbar$ is the Planck's constant.

Eq. 2.3 is similar in form to the well known Fowler-Nordheim equation for band-to-band tunneling in silicon, assuming a triangular potential barrier. The tunneling current density, J, can be written as [98],

$$J = CE^2 e^{-E_o/E} \tag{2.6}$$

where C and E_o are the constants corresponding to A_{kane} and B_{kane} of Eq. 2.3. Similar expressions have also been derived analytically to explain the gate-induced drain leakage (GIDL) currents [39, 99] and for B^2T-MOSFETs [64]. Depending on the bias conditions and device geometry, slight variations in the values of A_{kane} and B_{kane} are indeed observed. However, the basic *expression* remains the same. Since the aim of this work is not to determine the accurate values of A_{kane} and B_{kane}, using the existing model, the validity of the model for the tunnel FETs is investigated.

The current for the above mentioned GIDL phenomena is directly related to the gate bias, V_{GS}, and the solution can therefore be readily reduced to a 1-D problem. However, since the tunnel FET have a p-i-n diode configuration, a direct approach to solve the problem requires a solution of 2-D Poisson's equation as a function of both V_{DS} and V_{GS}, in order to calculate the p-n junction formed by V_{GS} for a given V_{DS}. The depletion width of this p-n junction would then give the tunnel barrier width, ω. Coupled with the tunnel barrier height, W_g, one will then need to solve Schrödinger's equation using proper approximations and tools. This approach becomes more complicated, as the free carrier concentration (majority or minority carriers, depending on the gate bias) is non-uniform across the channel.

Fig. 2.5 shows the simulated electron concentration, e_c, across the channel, close to and parallel to the Si-SiO_2 interface for the 2-D device geometry of Fig. 2.1, as a function of V_{GS}.

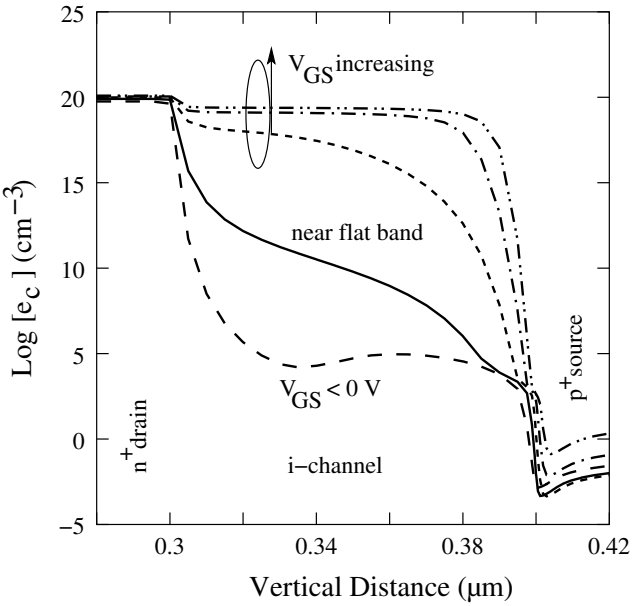

Figure 2.5: *Simulated electron concentration across the channel, close to the Si-SiO_2 interface, for a vertical tunnel FET, as a function of V_{GS}*

The channel length, L is 100 nm, and $t_{ox} = 2$ nm. The dopings in the p^+source and n^+drain is chosen to be 1×10^{20}cm^{-3}, while that in the channel is 1×10^{16}cm^{-3} n-type corresponding to the unintentional doping level during MBE growth.

It should be noted that the n-channel tunnel FET electrical parameters, like V_T and I_{on}, are a strong function of the doping profile [89] and doping smear-out effects [85] in the p-source region in the absence of the delta doped layer. However, in the current discussion, with a t_{ox} of 2 nm, abrupt and high doping profiles are chosen. Since epitaxy by MBE or low pressure chemical vapor deposition (LPCVD) techniques can be carried out at temperatures below 750^{o}C, sharp doping profiles can be achieved. The only high temperature step is the thermal oxidation for the gate oxide. Fig. 2.6 shows the simulated broadening of doping profiles using ATHENA of SILVACO [100] for our standard rapid thermal oxidation process for thin oxides (wet oxidation at 900^{o}C for 10 seconds) which yields a 3.8 nm oxide thickness. It is observed that the smear-out effect is not large. The effect of p-substrate (source) doping on the device electrical parameters will be discussed later in this chapter.

Thus, as it can be seen from Fig. 2.5, the solution of 2-D Poisson's equation itself would require analytical and numerical approach. For ideal flat-band conditions, e_c is exponentially varying from the p-source to n-drain end. This itself is quite complicated to solve for a p-i-n diode. Further, a small application of a positive (or negative) V_{GS} introduces a high degree of non-linearity in e_c.

In order to solve the above problem, a few assumptions are made to reduce the problem from that of both V_{GS} and V_{DS} dependence to a function of V_{GS} only. This can be done, as can see from the band diagrams of Fig. 2.7, the output characteristics of the tunnel FET, is a function of both V_{GS} and V_{DS} for low V_{DS} only[3]. As V_{DS} is increased, the device $I_{DS} - V_{DS}$

[3]For the time being, it is assumed that V_{DS} reaches saturation, and only V_{GS} matters. However, later in the thesis, using experimental results, it will be shown, that the expression thus derived, holds good for the

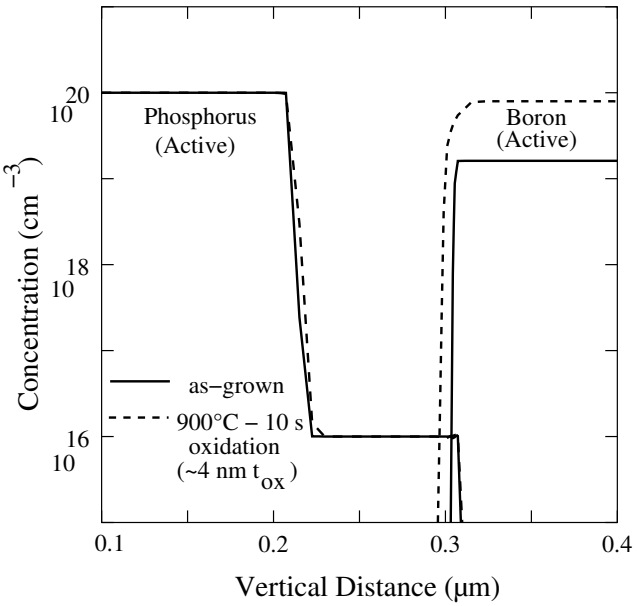

Figure 2.6: *2-D Simulated doping profile for the Si tunnel FET for our standard process flow for thin oxides reveal that the smear-out effect is not large.*

characteristics reaches saturation as the tunneling width is saturated with V_{DS}.

In Fig. 2.7 simulated band-diagrams for a tunnel FET close to the Si-SiO_2 interface, at $V_{GS} = 0$ V, and V_{DS} varying from 0 to 1.0 V are shown. It is clearly seen that V_{DS} has little dependence on the tunneling width, ω. It should be noted, that while the depletion width of the reverse-biased p-i-n diode increases with increase in V_{DS}, the tunnel width, which is gate controlled, is nearly independent of the drain bias. Hence, in the absence of the gate bias, the tunneling width is controlled by V_{DS}. Thus, the bulk p-i-n diode Zener breakdown limit is reached at a relatively *large* V_{DS} value. This is primarily due to the channel resistance. In Fig. 2.8 simulated maximum electric field, E_{max}, is shown across the tunneling junction, as a function of V_{DS} at $V_{GS} = 1.0$ V $> V_T$. Clear saturation behavior is observed. E_{max} is initially seen to increase and then reaches saturation.

When V_{GS} is applied, the tunneling width is controlled by the p^+n^+ junction formed by the inversion channel and the p^+source region. The tunneling currents are then dominated by V_{GS} at relatively low voltages. Thus, in the saturation region, where it can be assumed that the device performance is independent of V_{DS}, the effect of V_{GS} is investigated. In Fig. 2.9 the simulated band diagrams for a tunnel FET, at $V_{DS} = 1.0$ V, are shown as a function of V_{GS}. The lowering of ω with V_{GS} is clearly seen. This accounts for the exponentially increasing transfer characteristics.

This can be seen from Fig. 2.8 for E_{max} varying as a function of V_{GS}, at $V_{DS} = 1.0$ V (that is, in the saturation region). Further, it is observed that the p-i-n diode junction fields are much less then the p^+n^+ tunnel junction fields due to V_{GS}. Thus, for low V_{GS} when the reverse-biased p-i-n diode characteristics are dominant, a nearly constant E_{max} is observed. As V_{GS} is increased, E_{max} is seen to increase linearly with respect to V_{GS}. Thus, in the

tunnel FET parameters, even in the quasisaturation region, for any V_{DS} value.

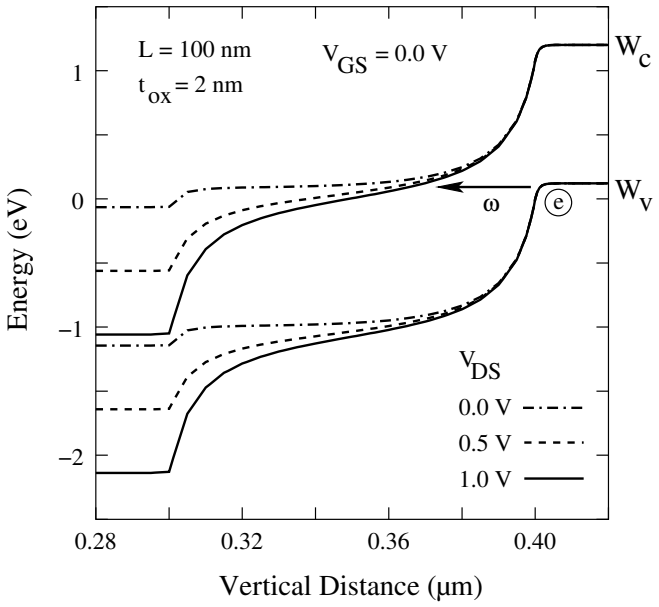

Figure 2.7: *Simulated band diagrams for the tunnel FET close to the Si-SiO_2 interface as a function of V_{DS} at $V_{GS} = 0$ V. $L = 100$ nm, $t_{ox} = 2$ nm.*

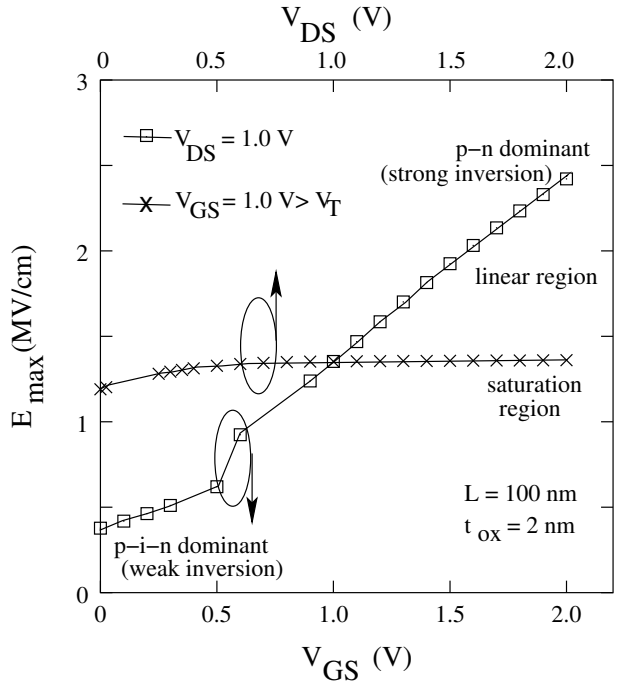

Figure 2.8: *Simulated maximum electric field, E_{max}, across the tunneling junction, of a tunnel FET, both as a function of V_{DS} (at $V_{GS} = 1.0$ V> V_T) and V_{GS} (at $V_{DS} = 1.0$ V, saturation region). Further, E_{max} essentially controls the device characteristics.*

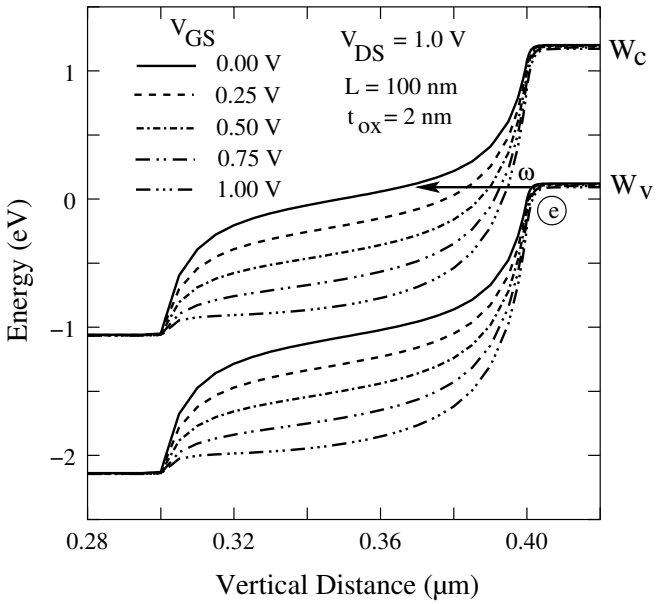

Figure 2.9: *Simulated band diagrams for the tunnel FET close to the Si-SiO_2 interface as a function of V_{GS} at $V_{DS} = 1$ V. $L = 100$ nm, $t_{ox} = 2$ nm.*

tunneling region E_{max} can be written as

$$E_{max} = DV_{GS}. \tag{2.7}$$

It should be noted that D, now is a function of V_{DS}, oxide thickness, t_{ox}, doping concentrations in the three regions, and channel length, L. In the saturation region D defines the device geometry parameter.

Thus, rewriting Eq. 2.3 in terms of V_{GS}, for

$$I_{DS} \quad \propto \quad G_{b2b}, \tag{2.8}$$

it can written as,

$$I_{DS} \quad = \quad A_{kane}D^2W_g^{-1/2}V_{GS}^2e^{-(B_{kane}W_g^{3/2})/(V_{GS}D)}. \tag{2.9}$$

A quick way to justify this would be to compare the equation with experimental results. The normalized drain current, $I_{DS-norm}$ is thus defined as,

$$I_{DS-norm} = I_{DS}/V_{GS}^2. \tag{2.10}$$

Taking natural log of the above equation, $I_{DS-norm}$ is written as,

$$Log\frac{I_{DS}}{V_{GS}^2} = Log\frac{A_{kane}D^2}{W_g^{1/2}} - \frac{B_{kane}W_g^{3/2}}{DV_{GS}}. \tag{2.11}$$

Thus, plotting $Log(I_{DS}/V_{GS}^2)$ with respect to $1/V_{GS}$, one would expect a straight line with a slope determined by B_{kane}/D, while the intercept giving $A_{kane}D^2$ for constant W_g. Fig. 2.10 the normalized I_{DS} as a function of inverse V_{GS} is plotted for the experimental data

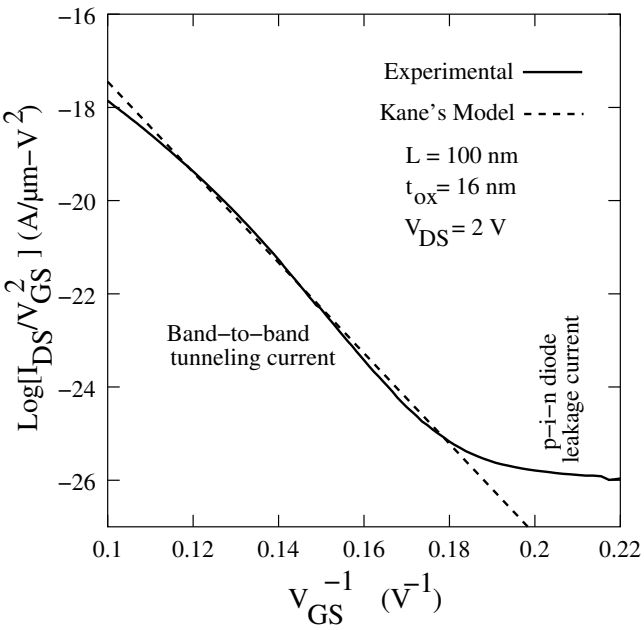

Figure 2.10: *Modified Kane's model (Eq. 2.9) fit with experimental results for n-channel tunnel FET (data corresponding to the device of ref. [86]).*

for the saturation region of the n-channel silicon tunnel FET corresponding to the device of [86] with $L = 100$ nm, $t_{ox} = 16$ nm. It can be seen that the modified Kane model fits the experimental data quite well in the saturation region[4]. Thus, justifying the approach used. Further, for a given device parameters, like source/drain doping concentrations, oxide thickness, t_{ox}, and bandgap, W_g, the value of D can be determined.

Fig. 2.11 shows the simulated band-to-band tunneling component, I_{b2b} and the total current I_{DS} as a function of V_{GS} for the device at $V_{DS} = 1.0$ V. For low V_{GS}, when the p-i-n diode characteristics are dominant (weak inversion region, corresponding to Fig. 2.8), the constant bulk p-i-n diode leakage current, I_{bulk}, is observed. The band-to-band tunneling probability, and hence the tunneling current, I_{b2b}, is low and does not add to I_{DS}. As V_{GS} is further increased (strong inversion), I_{b2b} becomes significant and I_{DS} starts to increase exponentially.

2.3.3 Device Simulation Models

Apart from the non-local Kane's model, the concentration dependent bandgap narrowing model is also included since highly doped source and drain regions are used, and tunneling has non-negligible dependence on the bandgap. Due to degenerate source and drain doping profiles, Fermi-Dirac statistics are used. Since the device characteristics are dominated by band-to-band tunneling current and impact-ionization related currents are negligible, for simplicity, the impact-ionization model is not included. For large drain biases and short-channel lengths, this may become important. However, any impact ionization related *hard* breakdown is not observed in our experimental tunnel FETs down to 25 nm channel length.

[4]In chapter 5 good agreement will be confirmed for an experimental p-channel tunnel FET with a t_{ox} of 4.5 nm and L of 70 nm.

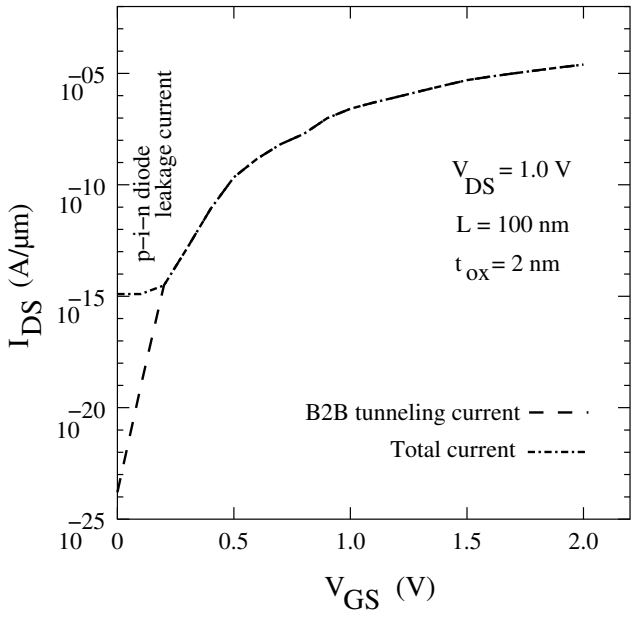

Figure 2.11: *Simulated transfer characteristics using the modified Kane's model (Eq. 2.9) for n-channel tunnel FET. The band-to-band tunneling component of the current as well as the total current are shown.*

As tunneling involves both electrons and holes, two carrier solutions are obtained. Gate tunneling leakage current models are also not included. The simulations are done for room temperature, $T = 300$ K.

2.4 Current-Voltage Characteristics

In this section, using the above mentioned models and tools, the silicon tunnel FET is investigated to study its scalability and usefulness with regard to the ITRS [68] requirements. Since for $L = 100$ nm, a t_{ox} of 2 nm is required for the conventional MOSFET to have the short-channel effects under control, the tunnel FET $I - V$ is investigated first with these parameters. The various regions of operation of the device are identified. Further, since the tunnel FET has a different current flow mechanism (tunneling) as opposed to the conventional MOSFET (diffusion and drift), the device electrical parameters, V_T and S, are redefined. The silicon tunnel FET is further subjected to the conventional MOSFET scaling rules and limitations are discussed. Both n-channel as well as p-channel behavior is investigated.

2.4.1 N-channel Tunnel FET

In this sub-section, the n-channel tunnel FET current-voltage characteristics is investigated for a technologically relevant device geometry with channel length, $L = 100$ nm and $t_{ox} = 2$ nm. The gate material is chosen to be n-polysilicon, while the dopings in the source (p^+) and drain (n^+) being uniform and abrupt at $1 \times 10^{20}\text{cm}^{-3}$. The channel doping is $1 \times 10^{16}\text{cm}^{-3}$ n-type corresponding to unintentional doping level during the MBE growth.

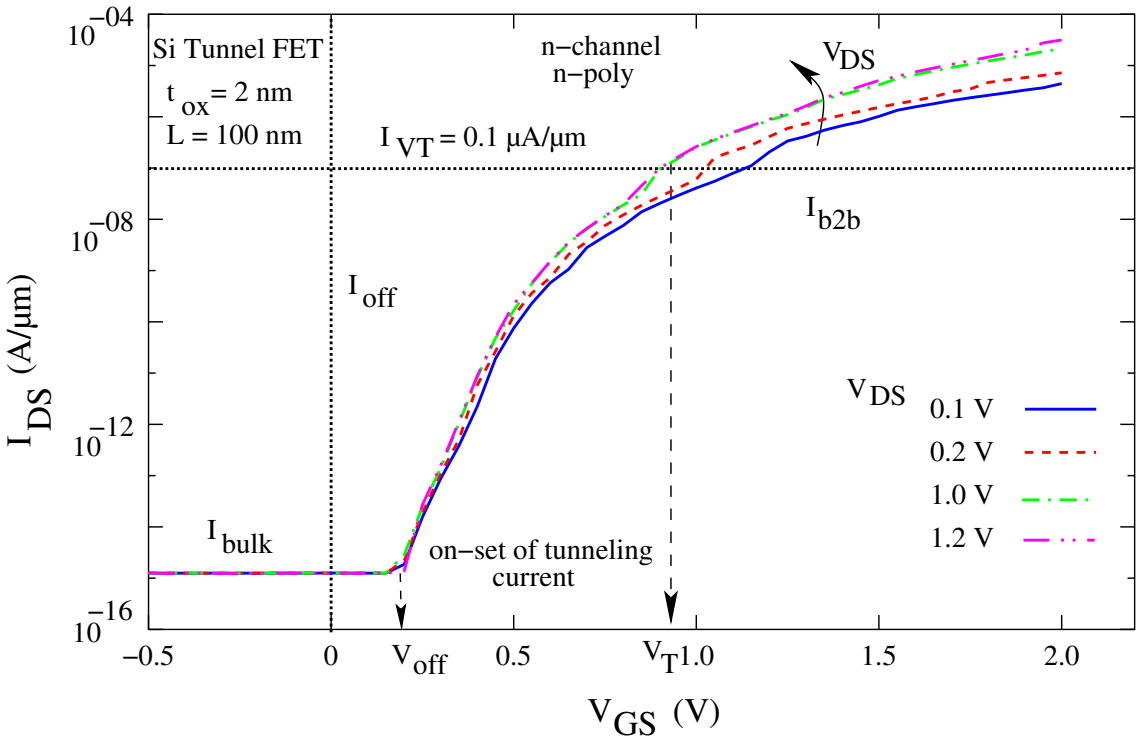

Figure 2.12: *Simulated transfer characteristics for a n-channel tunnel FET ($L = 100$ nm, $t_{ox} = 2$ nm). I_{bulk}, I_{b2b}, V_T and V_{off} are indicated.*

Input Characteristics

The n-channel transfer characteristics are shown in Fig. 2.12 as a function of V_{DS}. There is an initial V_{DS} dependence and than the curves coincide (saturation region) [5]. The threshold voltage V_T observed at $I_{DS} = I_{VT} = 0.1$ μA/μm is nearly 1 V while the on-current I_{on} at $V_{DS} = 1$ V $= V_{DD}$ and $V_{GS} = 2$ V for a 2 nm oxide thickness is 10 μA/μm. This is roughly 2 orders of magnitude less than the technology requirements. The leakage current I_{off} remains at the p-i-n diode leakage current value of 1 fA/μm at $V_{GS} = 0$ V. This is several orders of magnitude less than the ITRS requirements for a 100 nm technolog node [6]. The gate voltage, V_{off}, at which the I_{b2b} starts to domiate is shown in the figure.

The normalized drain current, $Log(I_{DS}/V_{GS}^2)$, as a function of V_{GS} is shown in Fig. 2.13 as a function of V_{DS}. Apart from linear behavior, parallel shifts in the curve for low V_{DS} is observed (exponential region of output characteristics) and then the curves coincide (saturation region). The linearity of the curves suggest good match with the modified Kane's model even for $t_{ox} = 2$ nm. For even thinner oxides non-linearity in the $E_{max} - V_{GS}$ relationship might occur. In the saturation region, the device geometry parameter, D, in Eq. 2.9 is

[5] It should be noted that the curves are not very smooth but show kinks in the characteristics. This is not due physical effects, but due to the simulation grid and bias points which are finite. It should further be noted, that the slight kinks here are different from those reported in [87]. They could also be due to the impact-ionization model [88] which cause *hard*-breakdown of the p-i-n diode leading to large 'jump' in the characteristics with small subthreshold swing. In the later case the device is operating as an I-MOS [58].

[6] It should be noted here, that I_{off} may be limited by the gate oxide tunneling leakage current which is not modeled here.

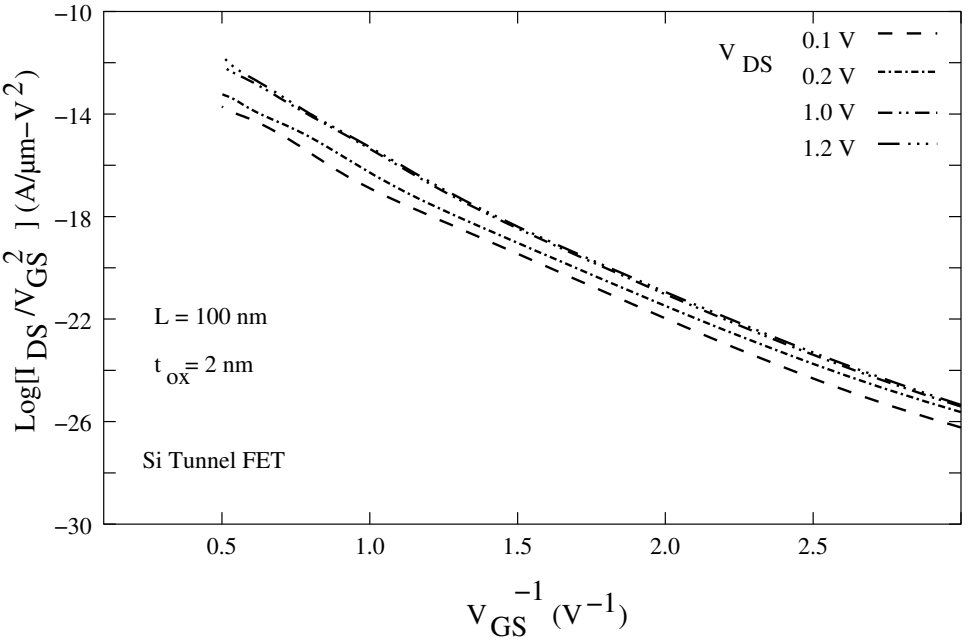

Figure 2.13: *Normalized I_{DS} as a function of inverse V_{GS} for a silicon tunnel FET ($L = 100$ nm, $t_{ox} = 2$ nm). The slope of the liner-fit gives the device geometry parameter, D, in the saturation region.*

determined by the slope of the linear fit.

Output Characteristics

The n-channel output characteristics is shown in Fig. 2.14. The various regions of operation are indicated. In the forward-bias, exponentially increasing normal p-i-n diode forward characteristics is observed. Furthermore, no gate dependence is observed. This is because, the probability of surface tunneling current is high only when the diode is reverse-biased. However, due to degenerate doping concentrations in the source and drain, even for low V_{DS} in forward-bias, the devices may show significant tunneling currents due to Esaki tunneling.

In the reverse-biased case, for $V_{GS} = 0$ V, reverse-bias p-i-n diode leakage current, I_{bulk}, of the order of 1 fA/μm is observed for $V_{DS} < 2$ V. As V_{DS} is further increased, p-i-n diode Zener breakdown leads to an exponentially increasing transfer characteristics. Since the source and drain dopings are high, the devices do not show hard breakdown corresponding the avalanche breakdown. Thus, in the absence of the gate bias, the tunneling widths are controlled by the drain bias at relatively large V_{DS} values. For $V_{GS} > 0$ V, I_{DS} initially increases exponentially, corresponding to the V_{DS} dependence region and then reaches saturation. Increase in I_{DS} with V_{GS} is exponential.

The output characteristics in the linear scale are shown in Fig. 2.15. In the saturation region, the output conductance, g_d, is found to be very small. There is no drain induced barrier lowering (DIBL), and the devices are virtually free from short-channel effects due to the saturation of the tunneling width, ω. The initial V_{DS} dependence comes from the lowering of the tunnel width which is inherent to the tunnel FET operation. Further, the drain dependence at the source end is minimized by the channel resistance. For low V_{GS},

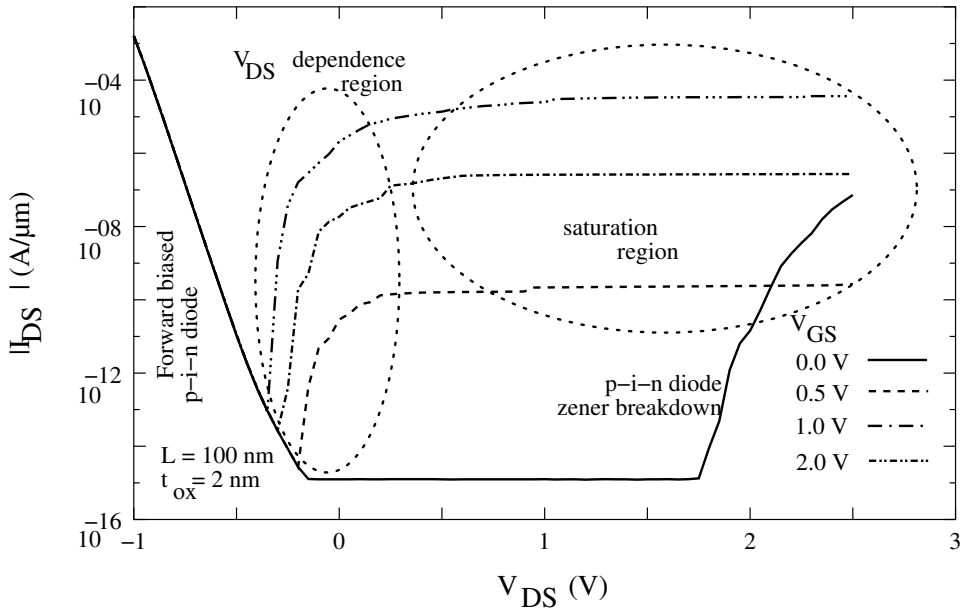

Figure 2.14: *Simulated output characteristics for an n-channel tunnel FET ($L = 100$ nm, $t_{ox} = 2$ nm). In the forward-bias, I_{DS} increases exponentially (diode current). In the reverse-bias, I_{DS} increases initially and then reaches saturation.*

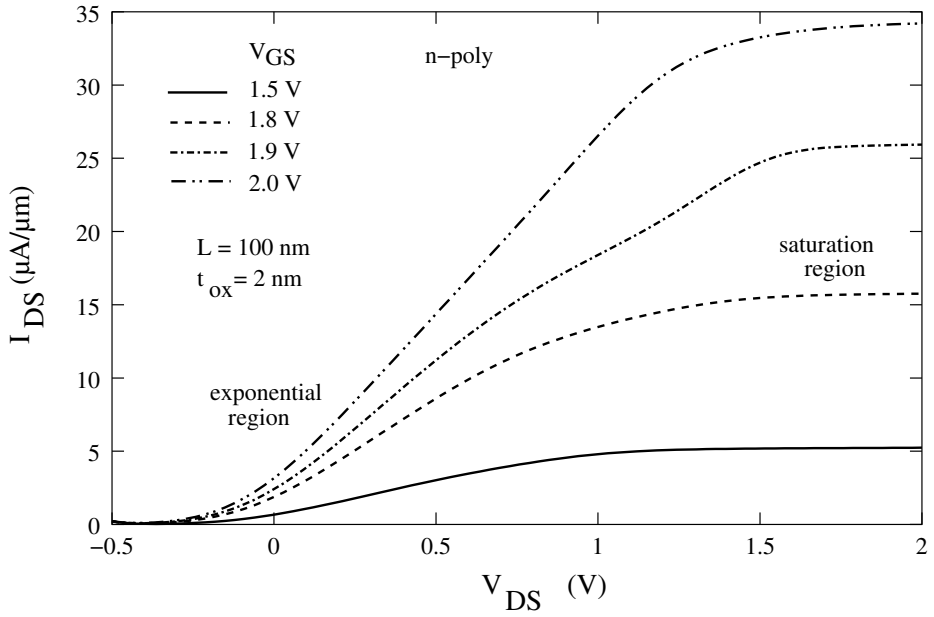

Figure 2.15: *Simulated output characteristics for the n-channel tunnel FET in the linear scale. Clear saturation region is observed.*

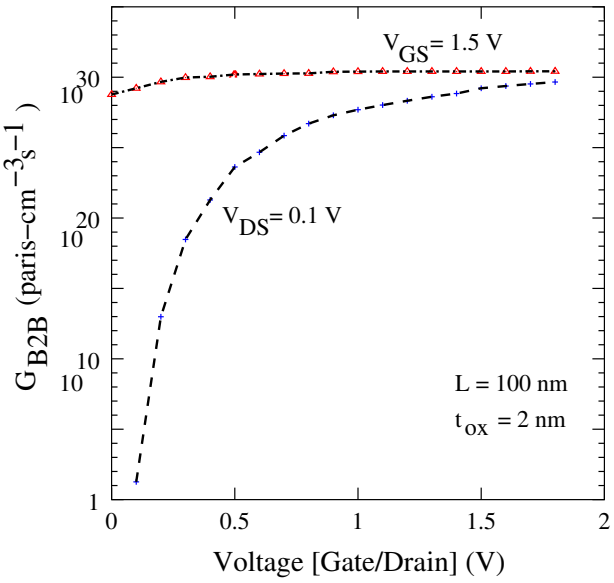

Figure 2.16: *Band-to-band tunneling generation rate as a function of both gate and drain bias, for a vertical tunnel FET.*

when the channel resistance is higher, saturation in the output characteristics is reached earlier. Increase in V_{GS} leads to a lower channel resistance. Thus, the drain dependence increases and saturation is achieved at a higher V_{DS} values. For thinner gate oxide thickness, the saturation behavior is further expected to improve as a result of a stronger gate coupling with the tunnel width, ω. It should further be noted, that the tunnel junction resistance is determined by both the abruptness and amount of dopants in the source region. A lower and smeared-out doping profile will lead to a poorer saturation behavior as the tunnel width will be lowered with increase in V_{DS}.

The transfer characteristics (at $V_{DS} = 0.1$ V) and output characteristics (at $V_{GS} > V_T$) are further investigated in terms of G_{b2b} (Fig. 2.16). As is clearly seen, G_{b2b} increases exponentially with increase in V_{GS} but saturates with V_{DS}.

2.4.2 P-channel Tunnel FET

In this sub-section, a discussion of the p-channel tunnel FET current-voltage characteristics is done. The device geometry and doping profiles are chosen to be the same as that for the n-channel tunnel FET. The gate electrode material is defined as p-polysilicon so as to have a high V_T for the n-channel operating mode, and low V_T for the p-channel operating mode. This is essential for the proper operation of the devices for CMOS technology. Since the tunnel FET is a gated p-i-n diode, for symmetric source and drain doping profiles, either n-channel or p-channel operating mode is 'on' with significant current when the other is 'off'. This will result in large leakage current in the device in the 'off' state. A possible solution has been proposed where the authors suggest the use of a lightly doped source (for p-channel) and lightly doped drain (for n-channel) [88]. However, a lightly doped contact will result in large contact resistance as well as gate-induced tunneling leakage currents. Thus, turning-off one operating mode by use of gate workfunction adjustment provides a better solution. In

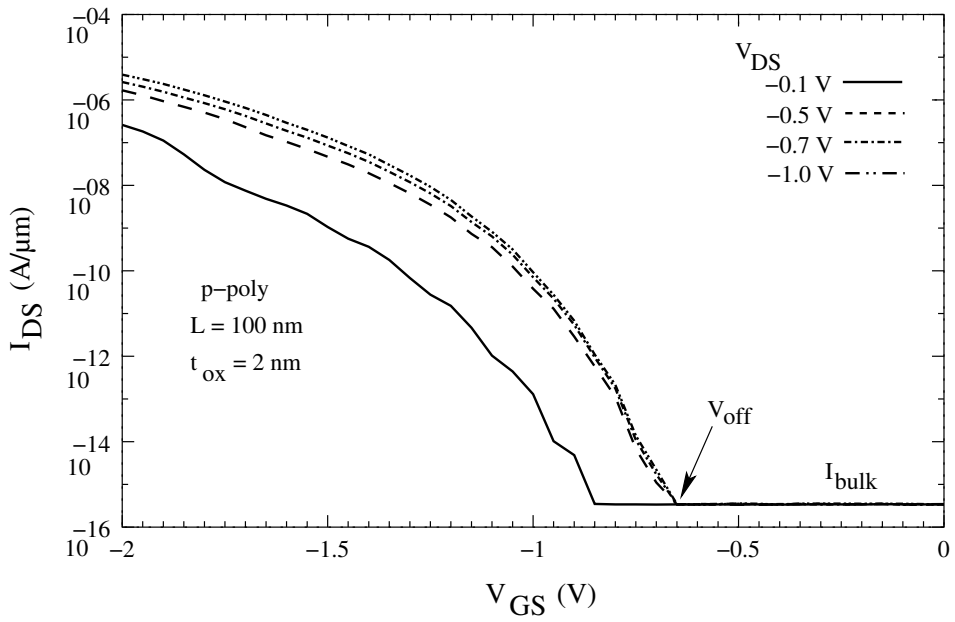

Figure 2.17: *Simulated transfer characteristics for a p-channel tunnel FET. P-poly is used as the gate electrode ($L = 100$ nm, $t_{ox} = 2$ nm).*

terms of technology, it will also requier a mask less, as both source and drain for both the n-channel as well as p-channel can be done simultaneously.

Input Characteristics

The transfer characteristics are shown in Fig. 2.17. Similar turn-on characteristics is observed, albeit at a higher V_T value of nearly 1.3 V. This is due to unintentional n-type doping in the i-channel. Saturation current of 5 μA/μm is observed. It should be noted, that the p-channel device with a p-polysilicon gate is not an optimum device but is shown here to illustrate the working principle. As can be seen from the figure, the device has a large V_{off} which can be further lowered by proper choice of gate material. This will further result in improved V_T and I_{on}.

Output Characteristics

Fig. 2.18 shows the p-channel output characteristics. The bias conditions are redefined so as to have a fixed V_{GS} at the tunneling junction. As expected, saturation behavior similar to the n-channel operating mode is achieved.

2.5 Tunnel FET Electrical Parameters

As it has been shown in the earlier sections, the tunnel FET current-voltage characteristics show a very different behavior as compared to the conventional MOSFETs. Of worth to note here, is the fact that while the conventional MOSFET has a diffusion current in the off-state (Eq. 1.4), and drift-diffusion current in the on-state (Eq. 1.6); the tunnel FET has

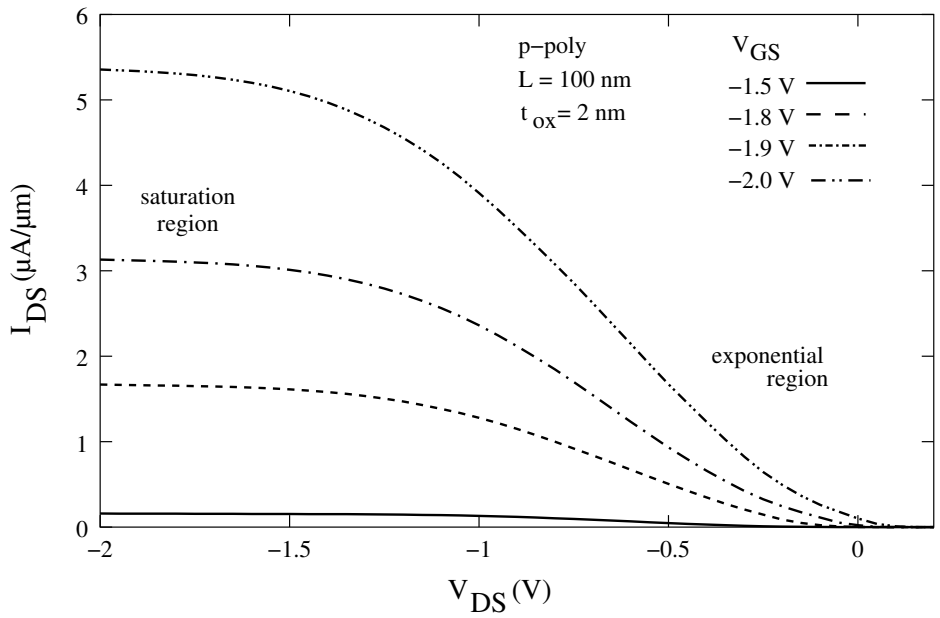

Figure 2.18: *Simulated output character for a p-channel tunnel FET. The characteristics show saturation behavior, similar to that n-channel operation mode.*

tunneling current for both the on-state as well as the off-state (Eq. 2.9) of operation. The bulk p-i-n diode leakage current of tunnel FETs is diffusion current and remains constant. Thus, different scaling rules and parameter definitions are needed for the tunnel FETs. In this section, the basic electrical parameters like threshold voltage, V_T, and sub-threshold swing, S are defined. Further, since the tunneling FET output characteristics has a exponential V_{DS} dependence region, for low V_{DS} and then saturation, the electrical parameters are defined in the saturation region of operation at $V_{DS} = V_{DD}$, the supply voltage. This is unlike the conventional MOSFET where the parameters are defined in the linear region of operation. However, this is not a disadvantage, as the devices are operated at $V_{DS} = V_{DD}$.

2.5.1 Threshold Voltage, V_T

For MOSFET circuit design and modeling, an accurate prediction of the threshold voltage, V_T is needed so as to determine circuit noise margins, speed and required node voltages. For a conventional MOSFET, V_T is the value of gate bias, V_{GS}, needed to induce a conducting channel at the surface [101]. Thus, for a long channel MOSFET, where the surface potential, ϕ_S, is assumed constant across the channel at low V_{DS}, the definition of V_T is based on the strong-inversion condition at which ϕ_S is twice of the bulk Fermi potential, ϕ_B.

$$\phi_S = 2\phi_B. \tag{2.12}$$

However, for experimental devices it becomes difficult to determine the surface and Fermi potentials, and thus the device V_T, accurately. Various alternative definitions and extraction methods of V_T have been proposed [102, 103]. Each of which comply by the three important criteria for its definition, viz: simplicity, unambiguity and consistency, and apply to different device geometry (L and W), and operating conditions. Some of the most commonly used V_T extraction methods are:

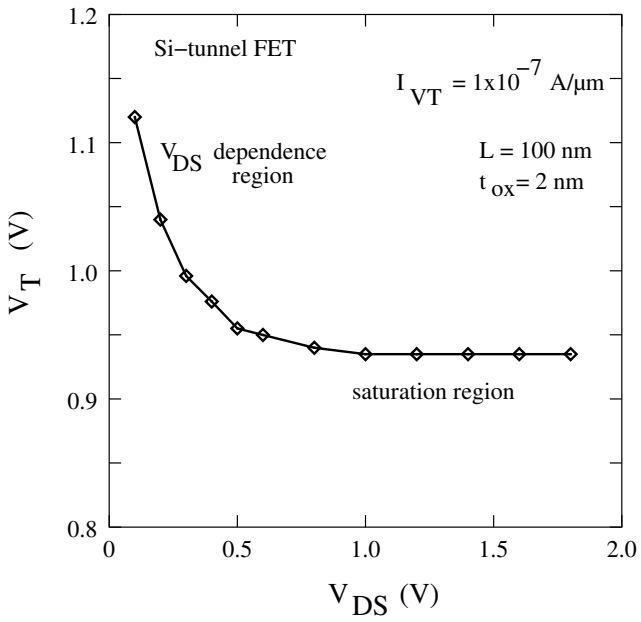

Figure 2.19: *Simulated V_T as a function of V_{DS} for a silicon tunnel FET by the constant current method similar to the one applied for conventional MOSFETs. I_{VT} =0.1 $\mu A/\mu m$ independent of L.*

(1) the channel current is linearly extrapolated to zero in the linear region of operation,
(2) the maximum transconductance, g_m, value method, and
(3) the constant current method at fixed $I_{DS} = I_{VT}$:

$$V_T = V_{GS} @ I_{VT} = I_{DS}\frac{W}{L}. \tag{2.13}$$

Since I_{DS} for a conventional MOSFET is a function of both L and W (Eq. 1.6), I_{VT} is normalized with respect to both L and W.

The working principle of a tunnel FET is very different. The highly non-uniform carrier concentration in the channel region renders the use of the surface potential definition meaningless, as both the surface as well as the Fermi potentials are varying in the channel region. Further, since the tunnel FET transfer characteristics is monotonically exponentially increasing, definitions (1) and (2) cannot be applied, as g_m is increasing exponentially for all values of V_{GS}. Thus, definition (3) is chosen for the tunnel FET V_T definition. Since I_{DS} is varying with parameters like t_{ox}, source-drain doping profiles, W_g and gate electrode workfunction, ϕ_m; V_T will thus also depend on these parameters. Fig. 2.19 shows the simulated V_T as a function of V_{DS}. For each V_{DS}, V_T is calculated at a constant

$$I_{VT} = 0.1\mu A/\mu m.$$

It should be noted, that I_{VT} here is normalized only with respect to W as the tunnel FET currents are independent of L up to very short-channel lengths. As can be seen from the figure, V_T is initially lowered with increase in V_{DS} and then reaches saturation. The lowering in V_T corresponds to the region where the tunneling widths are modulated with V_{DS}. Thus, the V_T value is defined in the saturation region of operation where V_T is independent of V_{DS}.

It should further be noted, that the lowering in V_T for low values of V_{DS} is quiet in contrast to the drain induced barrier lowring (DIBL) in conventional MOSFET. While DIBL is due to lowering in the diffusion barrier and increases with increase in V_{DS}, for tunnel FETs, the tunneling barrier is initially lowered, and then reaches saturation.

2.5.2 Subthreshold Swing, S

The sub-threshold swing is another electrical parameter of interest as it determines the turn-on turn-off ratio of the device. By definition, in the sub-threshold region, it is the change in V_{GS} needed to lower I_{DS} by one decade. As discussed in Section 1.1.3, it also determines the lower limit of the off-current, I_{off}, for a given V_T. Thus, the lowere S is, the better the device performance in terms of leakage currents is. For a conventional MOSFET, S is a constant and does not vary with V_{GS} or V_{DS}, and is a well defined parameter. The slope of the $I-V$ curve in the semi-logarithm plot gives the numerical value of S. However, as it will be shown below, and as expected, things are not the same for a tunnel FET.

Taking the log of Eq. 2.9 and differentiating it with respect to V_{GS}, for a tunnel FET in the saturation region, S is obtained as:

$$S = [\frac{dLog(I_{DS})}{dV_{GS}}]^{-1} = ln10\frac{V_{GS}^2}{2V_{GS} + B_{kane}W_g^{3/2}/D}. \tag{2.14}$$

It is seen, that unlike the conventional MOSFET, where the sub-threshold swing, S is a function of the thermal factor, kT/q; for a tunnel FET, to a first approximation[7], S is independent of kT/q. This is not unexpected, as tunneling currents are weakly dependent on temperature. However, since S depends inversely on W_g (weak dependence), it might show a weak temperature dependence due to the increase in bandgap with lowering of T. Thus, marginally improving at lower temperatures. S is also directly proportional to V_{GS} (strong dependence) and the device geometry parameter, $D = D(t_{ox}, N, L)$.

Since S depends strongly on V_{GS}[8], and degrades with increasing V_{GS}, it can be controlled by not only controlling the device geometry, D, but also the bias conditions. As S is lowered by lowering V_{GS}, it would imply that for very low V_{GS}, one can get very low S (large on/off ratio), ideally going to zero as V_{GS} goes to zero. This is explained in the following way. Considering a simple ideal case of a device with infinite channel length under flat band conditions.

[7] As will be shown later in the thesis, a weak positive temperature coefficient exists in the $I-V$ characteristics due to the dependence of W_g on T. However, S is nearly independent of T.

[8] It should be noted that this difference in the S comes from the different equations that describe the tunnel FET charateristics. While in the conventional MOSFETs the subthreshold current $I_{DS} \propto exp(V_{GS})$ (Eq.1.4), for the tunnel FETs, as derived above, it is proportional to $exp(-1/V_{GS})$ (Eq.2.9). Thus, even though in both the cases the current shows an exponential behavior, S shows very different behavior.

Similar behavior can be obtained from the band diagram Fig.2.9. To a first approximation considering constant tunneling barrier height (bandgap W_g) and effective mass $m*$ (it does not vary with applied bias),

$$I_{DS}(\omega) \sim e^{-\omega} \text{ and } 1/\omega \sim V_{GS} \tag{2.15}$$

Thus, taking a derivative of ω with respect to $\ln(I_{DS})$ and V_{GS}, we get

$$d\ln(I_{DS}(\omega)) \sim -d\omega, \text{ and } d\omega \sim -\omega^2 \cdot dV_{GS} \tag{2.16}$$

$$\text{Thus, } S(\omega) = \frac{dV_{GS} \cdot \ln 10}{d\ln(I_{DS})} \sim \frac{dV_{GS}}{-d\omega} \sim \frac{1}{\omega^2} \sim V_{GS}^2, \tag{2.17}$$

similar to the above derived Eq.2.14.

This would mean, a zero tunneling probability and only leakage currents. Application of a small V_{GS} would lead to a small but finite tunneling probability. That is when the device undergoes a transition from that of a p-i-n diode to that of a tunnel transistor. Thereby, leading to an infinitely large sub-threshold slope or *infinitesimal* swing. This again, is very unlike the conventional MOSFET behavior where S is a constant in the sub-threshold region and is further limited by the kT/q value. This gives the tunnel FETs an added advantage as they are scaled according to the ITRS [68] requirements. A sub-60 mV/dec swing leads to the possibility of optimizing the devices with a large I_{on}/I_{off} ratio even as they are scaled down.

The dependence of S on V_{GS} and W_g will be discussed in detail later in the thesis.

2.6 Band-to-band Tunnel (B^2T) FET and Surface Tunneling Transistor

Since the vertical tunnel FETs have a large gate overlap in the source/drain regions, and the device proposed here is operated at the limit of oxide breakdown due to high V_T values, the fields in both the oxide and the overlap regions are quite large. Further, this is true even for lateral devices which have significant gate-source overlap[9]. A discussion of the tunneling currents in the overlap region in surface tunnel FETs thus becomes necessary. Since the earlier tunnel transistors proposed had tunneling from the gate-source overlab region (B^2BT-MOSFET) [64, 65], a review of the two types of tunnel transistors proposed in literature is first done here. The following discussion is done only qualitatively in terms of band-to-band tunneling generation rate which determine the tunneling probability.

Three different cases are considered here for n-channel tunnel FET operation mode with the following doping profiles in the p^+ source region.

Case (i): A low source doping (3×10^{18}cm^{-3}) and no delta doped layer (Fig. 2.20). This corresponds to the B^2BT-MOSFET where a low source doping results in tunneling current due to the gate control. For a significantly lower doping profile, or a sufficiently high doping result in vanishing tunnel currents in the overlap region.

Case (ii): A low source doping (3×10^{18}cm^{-3}) and a highly doped δp^+ (1×10^{20}cm^{-3}) layer at the channel-source interface (Fig. 2.21), and,

Case (iii) a high source and delta doping of 1×10^{20}cm^{-3} (Fig. 2.23).

Oxide thickenss t_{ox} is chosen to be 2 nm, while channel length L is kept at 100 nm. The drain and channel dopings are kept at n-type 1×10^{20}cm^{-3} and 1×10^{15}cm^{-3}, respectively.

The band-to-band tunneling generation rate (probability), G_{b2b}, contours are plotted for each case at $V_{DS} = 1.0$ V (saturation region of operation) and $V_{GS} = 2.0$ V $> V_T$.

Thus, as can be seen in Fig. 2.20, in the absence of the delta layer which result in a very low source doping, the device exhibits large GIDL currents in the gate/source overlap regions. The gate-source bias causes large band-bending for band-to-band tunneling to take place. On the other hand, the doping at the p-source is not large enough to cause significant tunneling from the source to the inverted channel, and only a small component of the surface tunnel current is observed. Since the vertical surrounding gate structures have large gate overlap region, the parasitic GIDL currents can be quite large. The operating principle of

[9]For example, recently demonstrated lateral gated p-i-n diodes operation as Si-tunnel FETs [88, 135] and gated p-n junction diode operating as LITT [74].

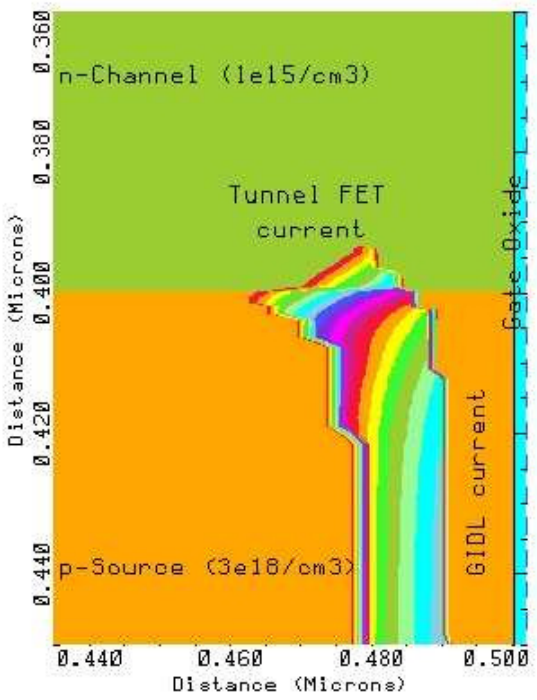

Figure 2.20: *Simulated G_{b2b} contours close to the Si-SiO_2 interface and tunnel junction in the absence of the delta layer ($V_{GS} > V_T$). The p^+ source doping in kept at $3{\times}10^{18}cm^{-3}$. As can be seen, large GIDL current is observed and is the dominant phenomena.*

the tunnel FET then is similar to that of [64] and the B^{2}T-MOSFET [65] where the tunnel current is of the GIDL origin.

Fig. 2.21 shows G_{b2b} contours for case (ii). As is seen, there is a significant lateral surface tunneling generation rate present in the channel region in addition to the GIDL currents of case (i). The doping in the delta layer and the source region will then determine as to which is the dominating effect. The currents are exponentially increasing with the maximum electric field across the tunnel junction, while the contribution due to the overlap region adds lineraly. Thus, if the junction fields are significantly higher, the GIDL currents may be negligible. Fig. 2.22 shows the simulated transfer characteristics for the tunnel FET with change in the substrate (source) doping, while a constant highly doped delta layer is used as a buffer. While significant variation in the tunnel FET parameters is reported with change in source-doping in the absence of the delta layer [85, 89], for this device, the increase in current is only by a factor of 2 for N_A increasing from $3{\times}10^{18}$cm^{-3} to $1{\times}10^{20}$cm^{-3}. As the high delta doped layer results in the p-i-n diode depletion width extending to only a few nanometers into the source, the substrate doping has little effect.

Similarly, G_{b2b} contours for a highly doped source region (case (iii)) reveal the complete absence of the GIDL currents and only surface tunnel currents are present (Fig. 2.23). Due to the high p-source doping, the gate overlap has little affect on the bands in the source. Further, the high delta doping results in a very narrow depletion width in the p-source. This is further confined mainly in the delta layer and the electric field falls rapidly to zero a few nanometers into the source (Appendix A). The maximum p-n junction electric field, E_{max}, thus, causes large surface tunneling currents.

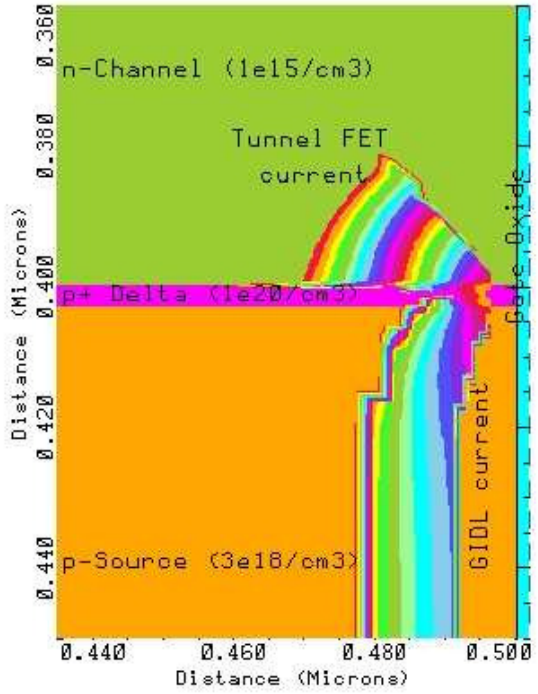

Figure 2.21: *Simulated G_{b2b} contours close to the Si-SiO_2 interface and tunnel junction with a δp^+ layer ($1\times10^{20}cm^{-3}$) and p^+ source $3\times10^{18}cm^{-3}$ ($V_{GS} > V_T$). Both the GIDL current and the lateral surface tunnel FET current is observed.*

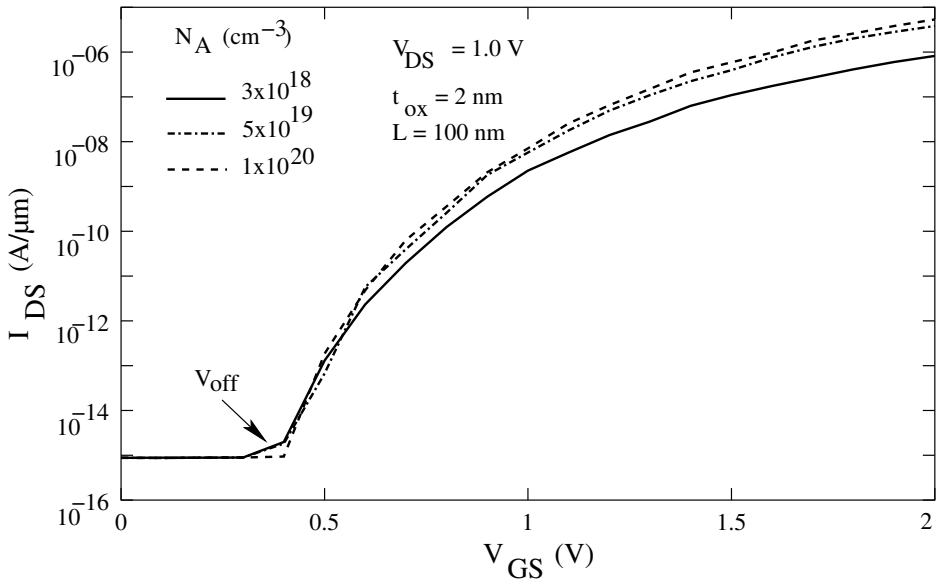

Figure 2.22: *$I_D - V_{GS}$ for a vertical tunnel FET with change in source doping, N_A at $V_{DS} = 1.0$ V, while a δp^+ layer is used as a buffer.*

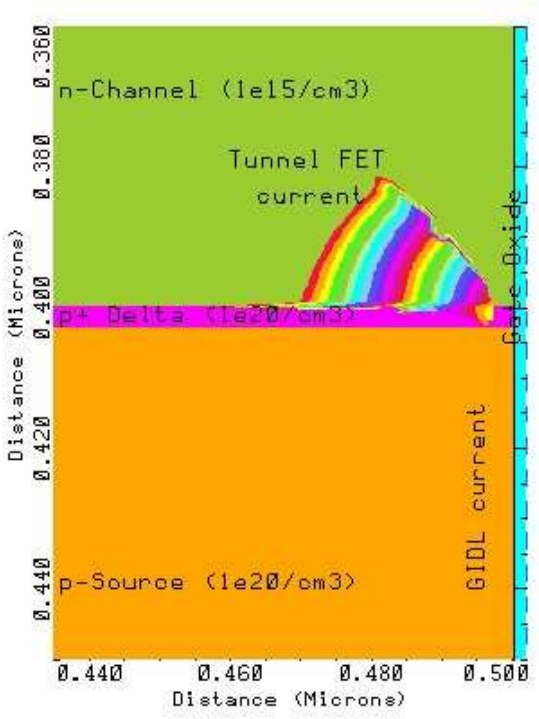

Figure 2.23: *Simulated G_{b2b} contours close to the Si-SiO_2 interface and tunnel junction with a δp^+ layer ($1\times10^{20}cm^{-3}$) and higher p^+ source $1\times10^{20}cm^{-3}$ ($V_{GS} > V_T$). The tunneling current in the gate-source overlap region is completely absent.*

It should also be noted here that the GIDL component of the current is expeced to be present for both forward-biased and reverse-biased diode. However, since for the n-channel operating mode, it is generated at the source end which is grounded, the drain dependence on the GIDL component is virtually screened by the large channel resistance, resulting in improved saturation behavior.

Thus, in general, a gated p-i-n diode operating as tunnel transistor will have both the components of the current. The source doping profile than becomes an important parameter in determining which is the dominant phenomenon. The on-current achieved for the B^2T-MOSFET at reasonable gate-source voltage is not high enough and the device fails to meet the technology requirements in terms of I_{on} and V_T. Further, tunneling from the source-gate overlap region is very critcal on the source doping and vanishes at sufficiently higher or lower doping levels. For low source doping, even though the gate bias can cause significant band-bending, the tunneling probability is low due to a large depletion width, which determines the tunneling width. For high source doping, even though the depletion width is small, the V_T is high and results in the potential drop acorss the oxide and not the silicon.

A higher source doping, on the other hand, results in an improved STT performace and hence improved on-current. Since the leakage current is determined by the p-i-n diode diffusion barrier, it is not a strong function of the source and drain doping. Thus, both the STT and the B^2T-MOSFET have similar I_{off}.

2.7 Summary

In this chapter, a discussion of the electrical characteristics of a homogeneous vertical Si-tunnel FET is done. The device shows several superior characteristics in comparison the the conventional MOSFET. An exponentially increasing transfer characteristics, saturation in the output characteristics, virtually free from short-channel effects as the current is determined by the tunneling junction, and ultra low leakage currents make this device ideal for low power analog and digital applications. Further, the i-Si channel is ideally intrinsic and the device parameters, like V_T, I_{on}, S and I_{off} are nearly independent of the doping in this region within the unintentional MBE doping level. Thus, the problem due to the the statistical fluctuation of dopant atoms in the channel is not a limiting factor to the tunnel FET scaling.

The applicability of the Kane's model for band-to-band tunneling in direct bandgap materials, is investigated for the silicon tunnel FET, and is found to be in good agreement with the experimental results. This is further used to understand and optimize the device electrical parameters.

Scaling the Si tunnel FET according to the ITRS predictions for the conventional MOSFET reveals that even though the parameters like V_T and S are scalable and improve with t_{ox} scaling, they are nearly independent of L. Further, the improvement is not significant and even the optimized Si tunnel FET fails to meet the technology requirements in terms of V_T and I_{on}. I_{on}, infact, is two orders of magnitude below the ITRS requirements. Thus, there is need for an additional parameter to both allow scaling and improve the tunnel FET performance. The effect of tunnel bandgap, W_g, modulation with SiGe, on the tunnel FET electrical parameters is thus investigated in the following chapter.

Chapter 3

Heterostructure Tunneling Junction: δp^+ SiGe Layer

Strained SiGe heterostructures have been found to be useful in the CMOS technology. Modification of the bandgap structure by use of the 4% lattice mismatch, leads to a lower effective mass for the electrons and holes [106]. This in turn, enhances the carrier surface mobility. In conventional MOSFETs this has been demonstrated for both n-channel as well as p-channel devices [107–109]. However, for the tunnel FETs, mobility is not a concerning factor. Further, improving the electron mobility by having strained SiGe channel for the tunnel FET will result in I_{on} enhancement by no more than a factor of 2. Furthermore, the increase in the p-i-n diode diffusion leakage current, which determines the I_{off} of the tunnel FET, will be exponential due to an increase in the intrinsic carrier concentration, n_i, in SiGe as,

$$n_i = \sqrt{N_c N_v} e^{-E_g/2kT} \tag{3.1}$$

due to the bandgap lowering. Since I_{on} for the silicon tunnel FET is 2 orders of magnitude less then the ITRS requirements, having a SiGe channel is neither sufficient in terms of gain in I_{on} nor is desirable due to an increase in I_{off}.

SiGe layers have been used in vertical MOSFETs to suppress the floating-body effects [110] and increase hot-carrier effects [111]. This has been achieved by modulating the material properties by using SiGe. Since, for example, impact ionization coefficients are larger in SiGe than in Si, incorporating SiGe at the drain end of vertical MOSFETs resulted in larger impact ionization and hence increased hot-carrier effects.

However, for tunnel FETs, critical tunneling parameters are the tunneling barrier width, ω, which, as discussed in the previous chapter, is determined by the device geometry, bias conditions (V_{GS} and V_{DS}) and doping profiles; and, the tunneling barrier height, which is a material parameter and is determined by the bandgap at the tunnel junction, W_g. The tunneling probability is an exponential function of both, and increases with lowering of ω and W_g. Since with pseudomorphically strained SiGe, the W_g can be lowered by several 100 meVs, in this chapter, the effects of having a pseudomorphically strained SiGe at the tunnel junction to lower W_g is investigated. As shown in Fig. 3.1, the δp^+ Si layer of the homogeneous tunnel FET is replaced by a pseudomorphically strained δp^+ SiGe layer.

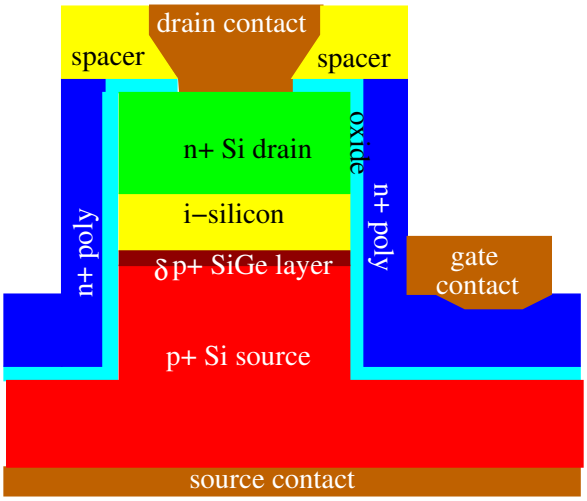

Figure 3.1: *Schematic representation of a tunnel FET with a 3 nm δp^+ SiGe layer at the source end.*

3.1 3 nm δp$^+$ SiGe layer

Strained SiGe on a Si substrate provides an opportunity to modulate the bandgap. Depending on the desired thickness, the Ge mole fraction, x, in SiGe, can be chosen. For a tunnel FET, band-to-band tunneling generation rate, G_{b2b}, is maximum and is confined to a very small region at the channel-source junction close to the oxide-silicon interface and falls rapidly to zero a few nanometers into the source. This is due to the fact that since the source is heavily doped and the channel is ideally intrinsic, the depletion width in the source extends to only a few nanometers. Thus, the electric field, E, vanishes 2-3 nm into the source (Appendix A). Therefore, an increase in the delta layer thickness is not expected to improve the device performance. In figures 3.2 the simulated G_{b2b} contours for a 3 nm and a 10 nm δp$^+$ SiGe layer tunnel FET respectively for n-channel operating mode ($V_{GS} > 0$ V) is shown. As can be seen, G_{b2b} is maximum and is confined to the high electric field region and vanish a few nanometers into the source. It should be noted, that this is true for a highly doped source region. In case of lightly doped source, the gate fields can still cause large tunneling currents due to interband tunneling along the interface, in the gate-source overlap region. Thus, in case of the device under consideration, a 3 nm δp$^+$ SiGe layer is sufficient to enhance the device performance.

The critical thickness, h_c of pseudomorphically strained SiGe on Si substrate is defined as the maximum layer thickness that can be deposited beyond which misfit dislocation array is energetically favored, leading to relaxation of the crystal lattice [112]. h_c depends on the Ge content, x, and the crystal orientation. Thus, the requirement of no more than a 3 nm SiGe layer is further advantageous, as the choice of Ge mole fraction, x, in pseudomorphically strained SiGe is not a limiting factor [106].

It should be further noted, that while considering this case, quantization effects in the 3 nm delta layer have not been taken into account and in all the discussions to follow, for the reverse-biased tunnel FET, the effect is not modelled. In case quantization plays a significant role in determining the device characteristics and degrades the performance, it would become

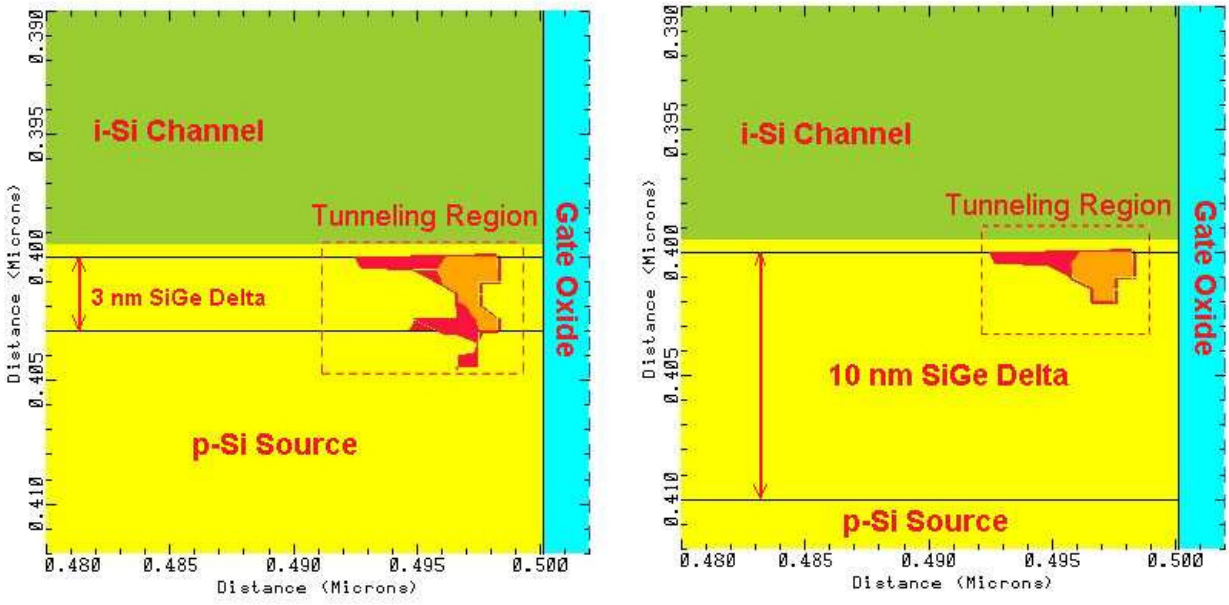

Figure 3.2: *MEDICI generated n-channel (positive V_{GS}) band-to-band tunneling generation rate, G_{b2b}, contours for (a) a 3 nm δp^+ SiGe layer, and, (b) a 10 nm δp^+ SiGe layer at the p-source end ($x = 0.5$). The cross-section is shown close to the Si-SiO_2 interface, at the channel-source junction. The p-source and delta layer have the same doping ($1{\times}10^{20} cm^{-3}$).*

necessary to increase the δp$^+$ layer thickness. This may limit the choice of Ge content, x, in SiGe.

3.2 Simulation Bandgap Parameters

The lattice parameters of a $Si_{1-x}Ge_x$ alloy are in general determined by the Vegard's rule which uses a linear interpolation of the parameters of the end-point elements Si and Ge [113]. However, deviations observed in the experimental data from the Vegard's rule have lead to a more precise determination of the parameters by use of parabolic or cubic interpolation.

The bandgap, W_g, for the strained energy bandgap model at $T = 90$ K in MEDICI is determined from the following equations [114].

$$\begin{aligned} W_g(x) &= W_g(90) - 4.0(W_g(90) - 0.950)x \quad , x \leq 0.25 && (3.2)\\ &= 0.950 - 0.66666(x - 0.25) \quad , 0.25 < x \leq 0.40 && (3.3)\\ &= 0.850 - 0.57500(x - 0.40) \quad , 0.40 < x \leq 0.60 && (3.4)\\ &= 0.735 - 0.43333(x - 0.60) \quad , 0.60 < x \leq 0.75 && (3.5)\\ &= 0.670 \quad , x > 0.75 && (3.6) \end{aligned}$$

Since simulations are done for temperature, $T = 300$ K, the bandgap at $T = 300$ K is calculated from the lattice temperature dependent energy bandgap model as follows [115].

$$W_g(x,T) = W_g(x,300) + \alpha[\frac{300^2}{300+\beta} - \frac{T^2}{T+\beta}] \qquad (3.7)$$

$W_g(x, 300)$ is the bandgap of $Si_{1-x}Ge_x$ at 300 K while $\alpha = 4.73\times10^{-4}$ eV/K and $\beta = 636$ K are constant parameters. At $T = 300$ K, the bandgap of SiGe is calculated using the silicon bandgap $W_g(0, 300) = 1.08$ eV.

In the simulations, the maximum Ge content, x, is chosen to be 0.5 as even at this value the ITRS requirements are fulfilled. The values of A_{kane} and B_{kane} (Eqns. 2.4 and 2.5) are in general functions of carrier effective mass, m_o, but are taken to be constants here. Since m_o is reduced in pseudomorphic strained SiGe, the tunneling probability is higher. Thus, the tunnel FET performance is further expected to improve with proper choice of A_{kane} and B_{kane}.

3.2.1 Band Diagrams with δp^+ SiGe Layer

As it has been discussed in section 2.3.2, smear-out of dopant atoms in silicon can be controlled in silicon. Further, for SiGe, it has been shown that the out-diffusion of boron can further be suppressed by using carbon [116] and fluorine [117]. Since the solubility of Boron in SiGe is higher than in Si, higher boron doping concentrations can be achieved for the SiGe delta layer. However, in order to compare the device electrical parameters of the heterostructure SiGe device, with those of the homogeneous Si device, the doping is kept constant and abrupt at $1\times10^{20}cm^{-3}$ corresponding to the Si delta and p-source doping. Figures 3.3 and 3.4 show the corresponding simulated band diagrams for the heterostructure tunnel FET with a pseudomorphically strained δp^+ $Si_{0.5}Ge_{0.5}$ layer, parallel and close to the Si-SiO_2 interface of the 2-D device geometry (Fig. 3.1). It is clearly seen that the valence band is raised relative to the conduction band. This could lead to several hundred meV lowering of the bandgap. Thus, lowering the tunnel barrier height at the tunnel junction. With increase in V_{GS} (Fig. 3.3), the tunnel barrier width is lowered, resulting in an exponential increase in the tunneling current, similar to that of the silicon tunnel FET. With lowering of bandgap, a stronger gate coupling is also expected, resulting in better saturation behavior for the SiGe tunnel FET. This is further confirmed from the band-to-band tunneling generation rate, G_{b2b} as shown in figures 3.5 and 3.6 for $x = 0$, 0.2 and 0.5. G_{b2b} increases several orders of magnitude for x increasing from 0 to 0.5 for all values of V_{GS}, leading to a higher current. However, it increases significantly even at $V_{GS} = 0$ V as the tunneling probability becomes significant due to the band bending. With increase in V_{DS}, G_{b2b} increases initially and then reaches saturation. The saturation behavior is further seen to improve with increase in x.

3.3 Electrical Characteristics

In this section, at the effect of tunnel bandgap modulation on the device current-voltage characteristics and parameters is investigated.

3.3.1 Current-Voltage Characteristics

Fig. 3.7 shows the simulated transfer characteristics of a tunnel FET with change in x from 0.1 to 0.5, at $V_{DS} = 1.0$ V. Channel length, L is 100 nm and oxide thickness, t_{ox} is 2.0 nm. A significant increase in I_{on} and lowering of V_T is clearly observed. While I_{on} is seen to increase from 10 $\mu A/\mu m$ for Si ($x = 0.0$) to 900 $\mu A/\mu m$ for δp^+ $Si_{0.5}Ge_{0.5}$ tunnel FET. V_T, on the other hand, lowers from nearly 1.0 V for $x = 0.0$ to 0.3 V for $x = 0.5$. Since the

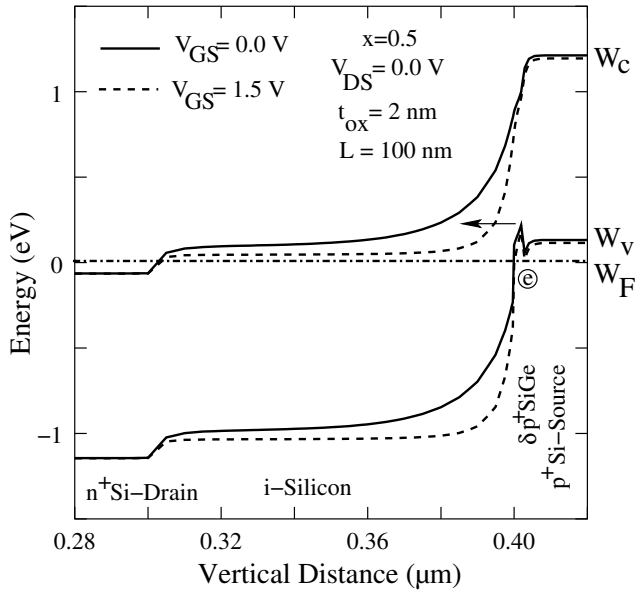

Figure 3.3: *Simulated band-diagrams for a δp^+ SiGe heterostructure tunnel FET ($x = 0.5$) for change in V_{GS}. A band off-set of a few 100 meV is clearly seen due to the raised valence band.*

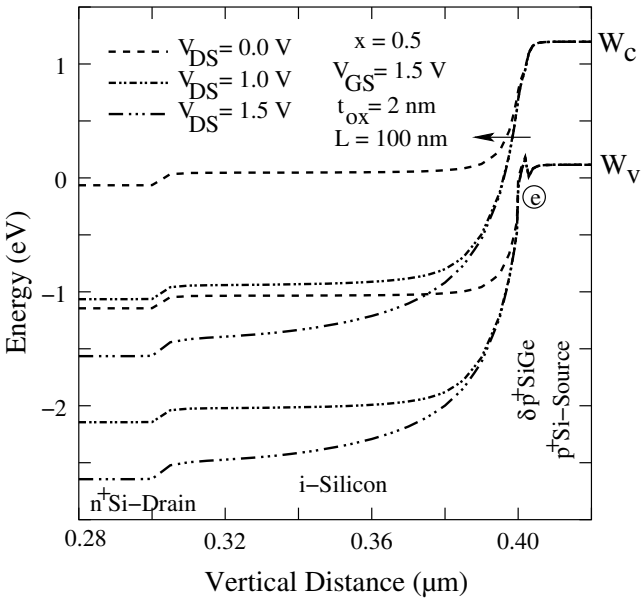

Figure 3.4: *Simulated band-diagrams for a δp^+ SiGe heterostructure tunnel FET ($x = 0.5$) for change in V_{DS}. Since the tunnel width is also lowered at similar biased condition, the SiGe tunnel FET is expected to show better saturation behavior.*

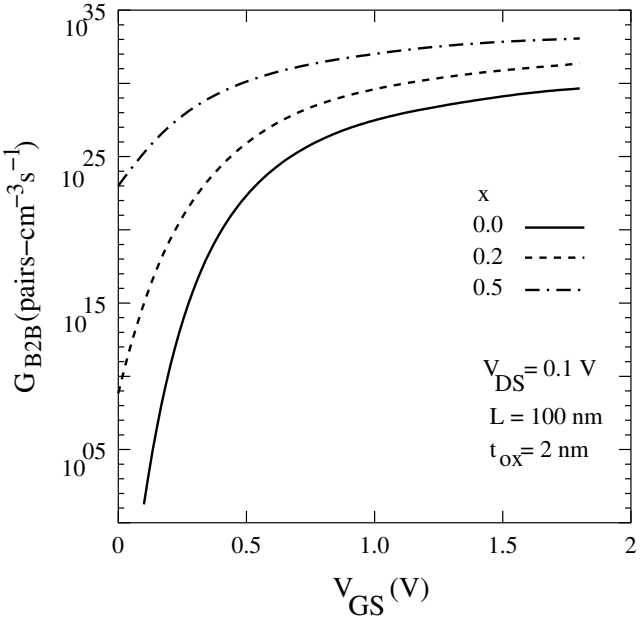

Figure 3.5: *Simulated G_{B2B} for x =0, 0.2, 0.5 with change in V_{GS} at $V_{DS} = 0.1$ V.*

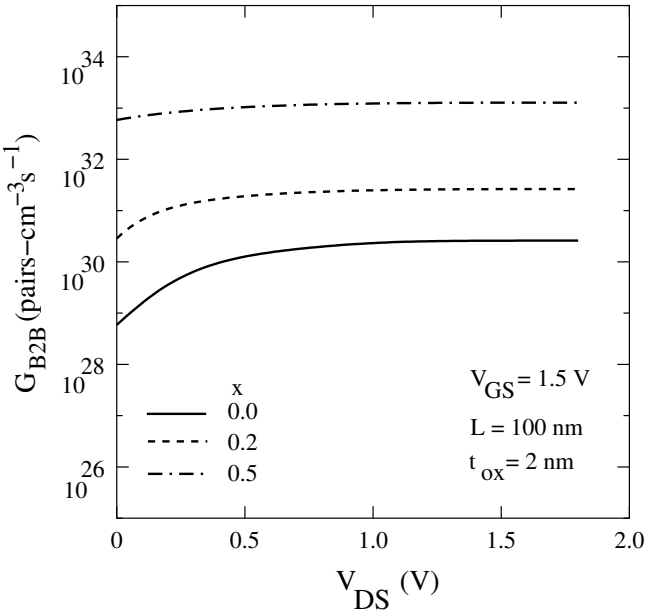

Figure 3.6: *Simulated G_{B2B} for x =0, 0.2, 0.5 with change in V_{DS} at $V_{GS} = 1.5$ V.*

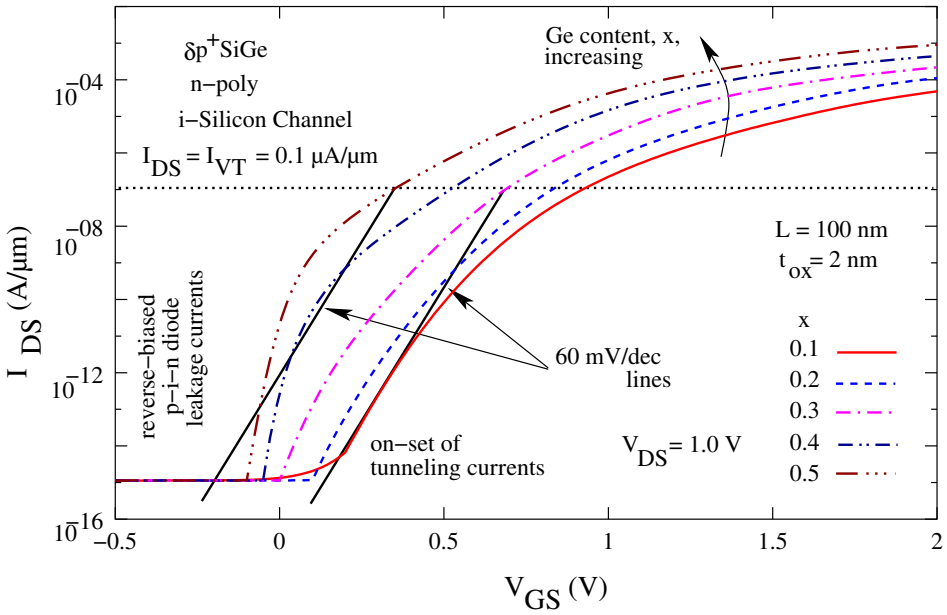

Figure 3.7: *Simulated n-channel transfer characteristics of the heterostructure tunnel FET as a function of Ge content, x, at $V_{DS} = 1.0$ V ($L = 100$ nm, $t_{ox} = 2$ nm). 60 mV/dec lines are drawn to compare the device turn off characteristics with that of an ideal conventional MOSFET.*

ITRS requirements of I_{on} for high speed applications is 900 μA/μm at a V_T of 0.3 V, a Ge mole fraction of 0.5 is sufficient to achieve this value. Fig. 3.9 shows the change in V_T as a function of Ge content, x.

For low power applications, I_{off} required is 1 pA/μA for the 100 nm node. As x is increased, the tunneling probability becomes significant even for $V_{GS} = 0$ V. While for $x = 0$ to $x = 0.3$, I_{b2b} remains below the bulk p-i-n diode current, I_{bulk}, at $V_{GS} = 0$ V, it becomes more dominant for $x > 0.4$. Thus, for higher values of x, I_{off} for a tunnel FET is dominated by I_{b2b}. Since the increase in I_{b2b} is exponential with x, the increase in I_{off} is also significant. A more clear picture of this is got from the I_{on}/I_{off} curve as a function of x (Fig. 3.10). For x increasing from 0 to 0.3, I_{on}/I_{off} increases. This is due to the fact that there is an increase in I_{on}, while I_{off} remains constant at I_{bulk}. However, as the Ge content, x further increases, there is a sharp drop in the I_{on}/I_{off} ratio as I_{b2b} starts to dominate. As the swing, S, for the tunnel FET is not a constant but degrades with increasing V_{GS}, the increase in I_{on} is not in proportion to the increase in I_{off}. In the following section, a discussion of the sub-threshold swing of the tunnel FETs, and its dependence on V_{GS} and W_g is done in detail.

3.3.2 Tunnel FET Sub-threshold Swing, S

Unlike the conventional MOSFETs, the tunnel FET swing is not only a device geometry parameter, but also a strong function of V_{GS} as it has been shown in Section 2.5.2. Since it is varying with V_{GS}, sub-threshold swing is not a constant. In order to have a quantitative comparison with the conventional MOSFET, the sub-threshold swing, S, is defined as an average value below threshold voltage, V_T. Thus, for the tunnel FET, I_{off} is defined as the constant p-i-n diode leakage current before the on-set of the tunneling current at $V_{GS} = V_{off}$.

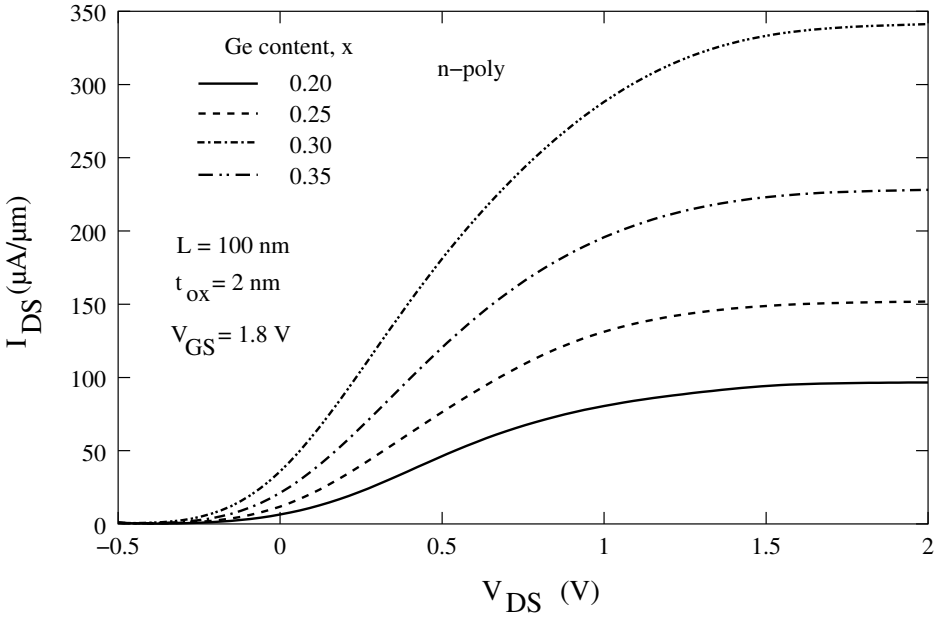

Figure 3.8: *Simulated n-channel output characteristics of the heterostructure tunnel FET as a function of Ge content, x, at $V_{GS} = 1.8$ V ($L = 100$ nm, $t_{ox} = 2$ nm).*

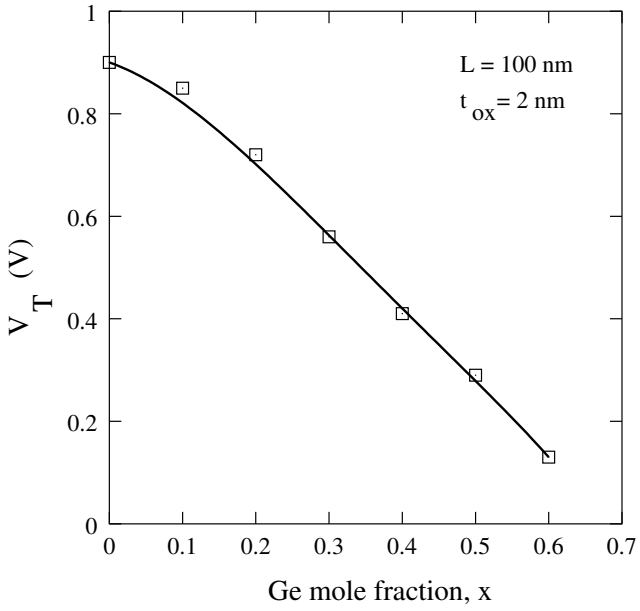

Figure 3.9: *V_T as a function of Ge content, x ($L = 100$ nm, $t_{ox} = 2$ nm). V_T is seen to lower significantly with increase in x and meet the technology requirements.*

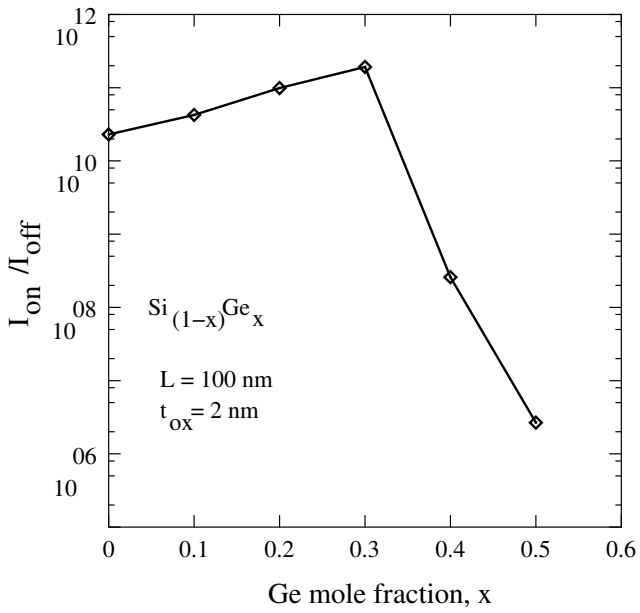

Figure 3.10: *I_{on}/I_{off} as a function of x. The ratio is seen to increase initially and then fall exponentially. The initial increase is due to the increase in I_{on} while I_{off} remains constant at I_{bulk}. For $x > 0.3$, I_{b2b} starts to dominate I_{off} and I_{on}/I_{off} is lowered significantly.*

Thus, V_{off} is the voltage at which the reverse-biased p-i-n diode characteristics undergo a transition to tunnel FET characteristics. Thus,

$$I_{off} = I_{bulk}, \tag{3.8}$$

$$\text{at } V_{GS} = V_{off}. \tag{3.9}$$

Ideally, one could call I_{off} as the tunnel FET leakage current under flat-band conditions. Further, by proper gate workfunction engineering one can always get a V_T shift to meet this requirement. Also, for any given device one can always choose $V_{off} = 0$ V complying with the conventional MOSFET definition of leakage current. Thus, the *effective sub-threshold swing*, S, for tunnel FETs, for I_{DS} decaying from I_{VT} to I_{off} can be written as,

$$S = \frac{V_T - V_{off}}{Log(I_{VT}) - Log(I_{off})}. \tag{3.10}$$

Fig. 3.11 shows the corresponding (effective) sub-threshold swing, S, as a function of Ge content, x and is seen to lower considerably with increase in Ge content, x. We further observe that it not only is lowered, but unlike the conventional MOSFETs, can be less than 60 mV/dec at room temperature.

To have a quantitative insight as to what in means in terms of device performance, 60 mV/dec lines corresponding to the ideal conventional MOSFET are plotted in the $I_{DS} - V_{GS}$ characteristics as a function of Ge content, x, as shown in Fig. 3.7. As is clearly seen, for $x = 0.3$ corresponding to effective $S > 60$ mV/dec, the tunnel FET performance is worse than that of the corresponding ideal conventional MOSFET. Similarly, for $x = 0.5$ corresponding to an effective $S < 60$ mV/dec, the tunnel FET performance is much better than that of the

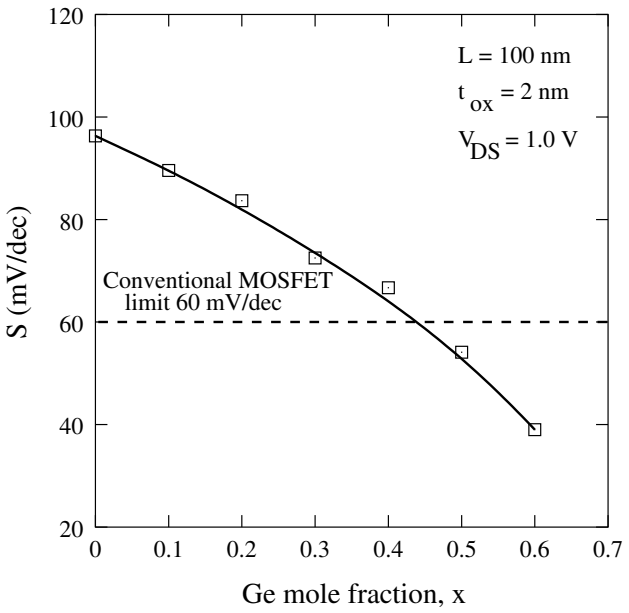

Figure 3.11: *Swing, S, as a function of x. Since S is a strong function of V_{GS}, average S is shown for change in I_{DS} from I_{bulk} to I_{VT} value. As is seen, average S can be less then 60 mV/dec for the tunnel FETs.*

ideal conventional MOSFET. Thereby, significantly improving the performance [1].

The sub-60 mV/dec effective swing for tunnel FETs, not limited by the thermal factor, kT/q, is not unexpected as interband tunneling is a weak function of temperature. In silicon, band-to-band tunneling is phonon-assisted by emission of phonons. Thus, the tunnel FET current-voltage curves are expected to show weak temperature dependence. This will be confirmed later in the thesis with experimental results. Thus, swing, S, for the tunnel FET is therefore, also expected to have a weak temperature dependence.

3.3.3 'Spot' Value of Swing, S

Alternatively, swing for tunnel FETs can be considered as a 'spot' value for any given V_{GS}. 'Spot' value of S at constant V_{GS} increases with increasing Ge content, x. However, calculating it at a constant V_{GS} is not likely to give a good measure of the device electrical parameters, as the device V_T and supply voltage change with scaling, doping density and profile, and W_g. Choosing S at the V_T value, it is lowered with increasing Ge content, x as expected, since V_T is lowered with increasing Ge content, x. However, the values of S are now much higher. This is shown in Fig. 3.12 where the 'spot' value of swing, S, at the V_T value and the effective subthreshold swing are shown.

We now look in detail the dependence of S on V_{GS} and bandgap, W_g for a fixed device geometry parameter, D. Fig. 3.13 shows schematically the band diagram with pseudomorphically strained SiGe at the p-source end. As is seen from the figure, there are two

[1] A sub-60 mV/dec room temperature swing has also been very recently experimentally demonstrated in carbon nanotube (CNT) MOSFETs operating in the band-to-band tunneling regime (ambipolar region) by IBM [118]. However, till date, an experimental sub-60 mV/dec swing has not been observed in gated p-i-n tunnel FETs in any material system. This is the first simulation observation of such a phenomenon.

consequences: along with the bandgap lowering at the tunnel junction, it is observed that the tunnel width is lower for SiGe than for Si at constant V_{GS}. As the Ge content, x is increased, the valence band is raised accordingly. Thus, the tunnel width is further reduced. As it is shown below, the lowering of tunnel width plays a significant role in determining the tunnel FET characteristics.

Since V_T for tunnel FETs is determined by the constant current method at $I_{DS} = I_{VT}$, lowering of tunneling barrier width, ω, with increase in x, significantly raises the tunneling probability, and hence the tunneling current at similar bias conditions. This lowers the device V_T considerably. Rewriting Eq. 2.14 for S as a function of V_{GS} and W_g,

$$S = \frac{ln10.V_{GS}^2}{2V_{GS} + B_{kane}W_g^{3/2}/D}. \tag{3.11}$$

it is seen that S is directly proportional to V_{GS} (strong dependence) and D, and inversely proportional to W_g (weak dependence). Since S is a strong first order function of V_{GS} and weak function of W_g, the device improvement is a result of ω lowering. This would further imply that for very low V_{GS}, one can get a very low S (large I_{on}/I_{off} ratio), ideally going to zero as V_{GS} goes to zero. This is explained in the following way, considering a simple ideal case of a device with infinite channel length under flat band conditions. This would imply a zero tunneling probability and only leakage currents. Application of a small V_{GS} would lead to a small but finite tunneling probability. That is when the device undergoes a transition from that of a reverse-biased p-i-n diode to that of a gate controlled surface tunnel transistor. Thereby, leading to an infinitely large slope or infinitesimal swing.

Further, from Eq. 3.11, it is also seen that at constant V_{GS} lowering of W_g would imply an increase in S, that is degraded performance. However, the (average) effective sub-threshold swing is seen to improve (lower) with increase in x. To investigate this in more detail, Fig. 3.14 shows the 'spot' value of S as a function of V_{GS} for Ge content, x, varying from 0 to 0.5. The 'spot' value of S at each V_{GS} is extracted from the simulated $I_{DS} - V_{GS}$ curve for each x value at $V_{DS} = 1.0$ V. The strong dependence of 'spot' S on V_{GS} is clearly seen. Also, for low V_{GS}, it is seen that S can be very small, tending to zero *irrespective* of x value. Further, the degradation of 'spot' S with W_g at *constant* V_{GS} is also observed. This is consistent with Eq. 2.14.

It should therefore be noted, that an effective sub-60 mV/dec sub-threshold swing for tunnel FETs is not only a material parameter, viz as shown for SiGe here, but a tunneling effect phenomena. The effect is observed clearly for the SiGe tunnel FETs due to stronger gate-tunnel barrier width coupling. It should therefore be possible to optimize the Si tunnel FET itself, by proper choice of the device geometry parameter D in Eq. 2.14, to have a better gate control and achieve an effective room temperature sub-threshold swing of less then 60 mV/dec.

Coming back to the problem of effective S lowering with increasing Ge content, x, the band diagrams at the tunnel junction are investigated more closely. Thus, in Fig. 3.13, the band diagrams with SiGe delta p^+ layer are shown schematically. Apart from the bandgap, W_g lowering, it is observed that since the valence band is raised, the tunnel barrier width ω is also significantly lower for the SiGe heterostructure device than for the Si homogeneous device, under similar bias conditions. This lowering in ω results in a stronger coupling between the gate bias and the tunnel junction, resulting in improved performance and swing. Further, this also accounts for the significant lowering of V_T with increasing Ge content, x.

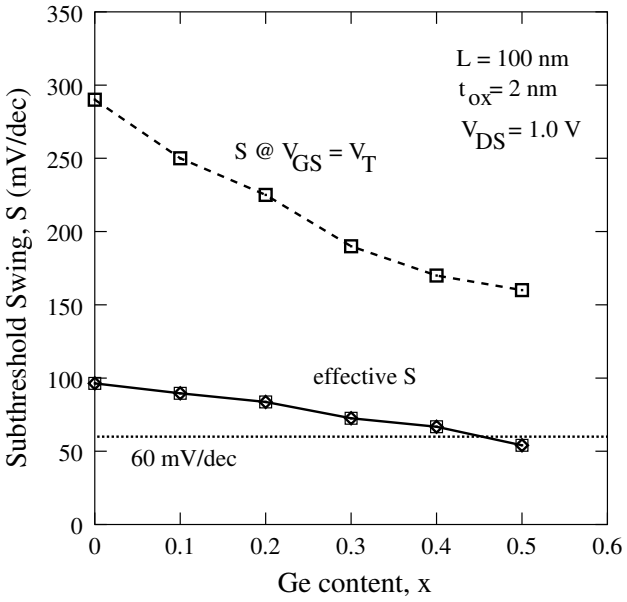

Figure 3.12: *'Spot' value of swing, S, at $V_{GS} = V_T$, and the effective subthreshold swing for the n-channel heterojunction tunnel FET. Both these values are seen to lower with increase in Ge content, x.*

As I_{DS} is falling faster than exponential below V_T, V_{off} does not scale as much as V_T for each x value. Thus, from Eq. 3.10, for fixed I_{VT} and I_{off}, $V_T - V_{off}$ is decreasing with increasing x. This leads to a significant lowering in effective S as x increases.

3.4 Asymmetry in n-channel and p-channel SiGe Tunnel FET Performance

The above discussion is done about the n-channel operating mode of the heterojunction tunnel FET. This is because the tunnel height and width has been modulated at the p-source end. Thus, the p-channel performance remains unaffected. Further, as it has been shown that the improvements in the device performance is not a direct consequence of the tunnel barrier height lowering, but an indirect consequence of the tunnel barrier width lowering. This results in an asymmetry in the heterostructure tunnel FET performance. As with pseudomorphically strained SiGe, *only* the valence band is raised relative to the conduction band, simply inserting a pseudomorphically strained n^+ SiGe delta layer at the n^+drain end is not going to give the desired improved performance. Since, even though the bandgap (tunneling barrier height) is lowered, the tunnel width ω, now determined by the valence band in the channel and the conduction band in the drain remains unaffected. Further, it may lead to a degradation in the overall performance as S degrades with lowering in W_g. Thus, figures 3.15 and 3.16 show the simulated band diagrams for the p-channel tunnel FET operating mode with and without 3 nm δn^+ SiGe layer at the n^+ drain end, respectively. As is clearly seen, even though the tunneling barrier height, W_g is lowered, the tunnel barrier width, ω remains unaffected.

Thus, for a p-channel tunnel FET, a different optimization scheme is needed.

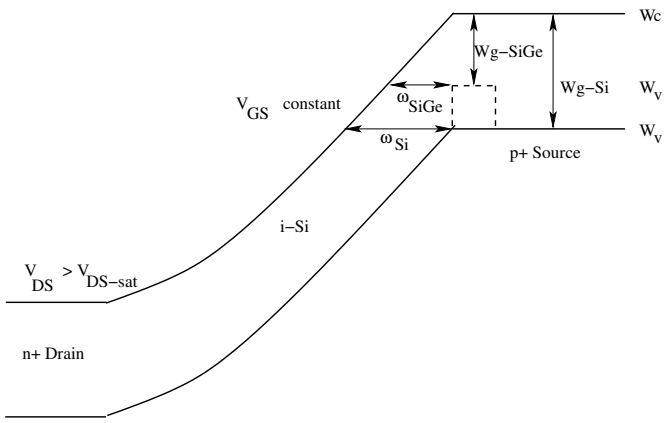

Figure 3.13: *Schematic representation of the band diagrams with SiGe delta layer. Two consequences are observed here. Apart from tunnel barrier height lowering, tunnel barrier width is also lower for a given bias conditions.*

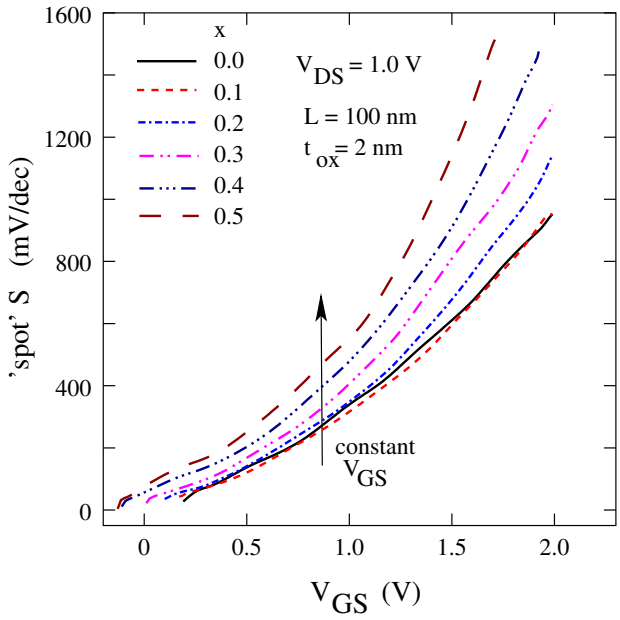

Figure 3.14: *'Spot' value of swing as a function of V_{GS} for Ge content, x, varying from 0.0 (Si only) to 0.5. As is seen, unlike the conventional MOSFET, S is a strong function of V_{GS} and bandgap, W_g, for a given device geometry determined by the parameter D.*

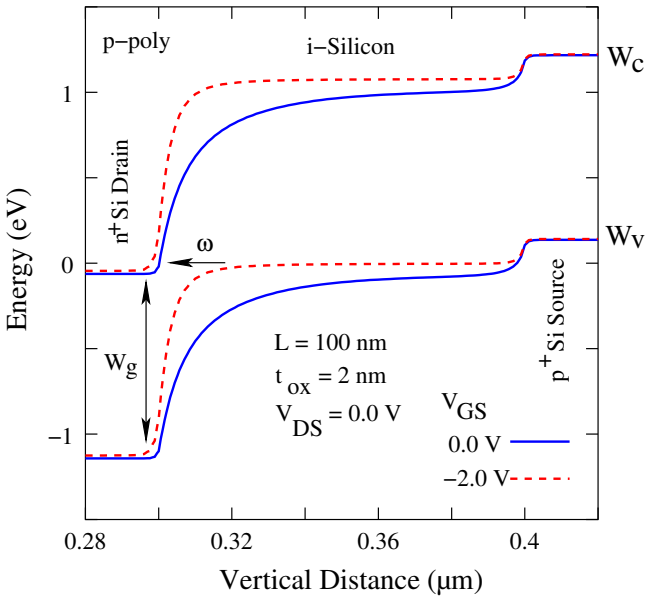

Figure 3.15: *Simulated band diagrams for a Si homogeneous tunnel FET for p-channel operation mode. The tunnel width is determined by the valence band edge in the channel and the conduction band edge in the n^+ drain. (P-poly is used as the gate electrode).*

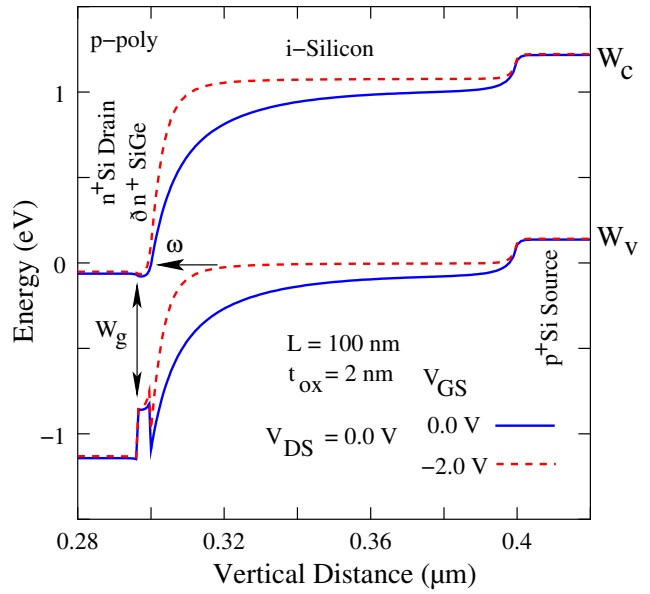

Figure 3.16: *Simulated band diagrams for p-channel tunnel FET operation mode with a highly doped δn^+ SiGe (Ge content, $x = 0.5$) layer at the n^+ drain end. Even though the bandgap, W_g is lowered, the tunnel width remains unaffected.*

3.5 Forward Biased Diode

In this section, we briefly discuss, by means of 1-D quantum mechanical (QM) device simulator, Nano Electronic MOdelling tool, (NEMO) [119], the effects of having a δp^+ SiGe layer on the forward biased characteristics of the tunnel FET. Since this is not the aim of the present thesis, the effects have not been investigated in detail and only qualitative studies have been done.

Forward-biased Esaki tunneling, resulting in a negative differential conductivity, has been observed in lateral gated p-i-n diodes both at low temperatures as well as high temperatures [76,77]. Resonant interband tunneling has been observed in Si/SiGe p-n junction diodes [120], while multiple resonant peaks have been observed in III-V compunds [121, 122].

Fig. 3.17 show the simulated band with the resonant state with a δp^+ silicon layer at the p-source end. The drain is degenerately doped, which result in the Fermi level lying inside the conduction band (as shown in the figure). As only 1-D simulations are done, in order to study the effect of gate bias, a small 'i'-Si region of less than 10 nm is chosen. This results in sufficient tunneling probability for electrons to tunnel from the degenerate conduction band into the valence band. When the diode is forward-biased, for small increase in V_{DS}, the tunneling current increases, as the density of states increases. For V_{DS} greater than the equilibrium Fermi level, it reaches a maximum, and then falls to zero (Esaki tunneling). The current-voltage curve for this device is shown in Fig. 3.18 for doping varying in Si-source. It can further be seen that the source doping has little effect on the diode $I-V$ characteristics. Further, the peak current is observed at below 0.1 V, corresponding to the Esaki tunneling.

Fig. 3.19 show the simulated band diagram for the heterostructure tunnel junction with SiGe (Ge content, $x = 0.8$). The choice of $x = 0.8$ is made only for clarity, and a constant effective mass is used for the simulations. This results in the large band-offset in the device. Quantization effects result in multiple resonant states (hole sub-bands) in the delta layer. Thus, the simulated forward current shows multiple peaks corresponding to the two states for the device. Further, the peak current density, as well as the peak-to-valley ratio are both seen to increase with increasing Ge content, x.

It should therefore, be noted, that for large L (> 10 nm in silicon), room temperature Esaki, or resonant interband tunneling for gated p-i-n diodes is improbable as it would require a very strong inversion of the channel. The forward-biased peaks in the differential forward current, observed for the vertical structures will be discussed with experimental results in chapter 5.

3.6 Summary

The tunnel FET based on silicon as discussed in the previous chapter, showed some superior properties in comparison to the conventional MOSFET. However, it failed to meet the technology requirement in terms of the on-current. In this chapter it has been shown, by means of 2-D computer simulations, that modulating the tunnel barrier height and width with SiGe in the δp^+ layer of the tunnel FET, gives us an additional parameter to improve and control the tunnel FET characteristics and parameters. In addition to achieving the technologically required V_T and I_{on}, it is also observed that the effective sub-threshold swing for the tunnel FETs is not limited to the room temperature thermal limit of 60 mV/dec.

The non-scalability of S for conventional MOSFETs limits the maximum I_{on}/I_{off} ratio

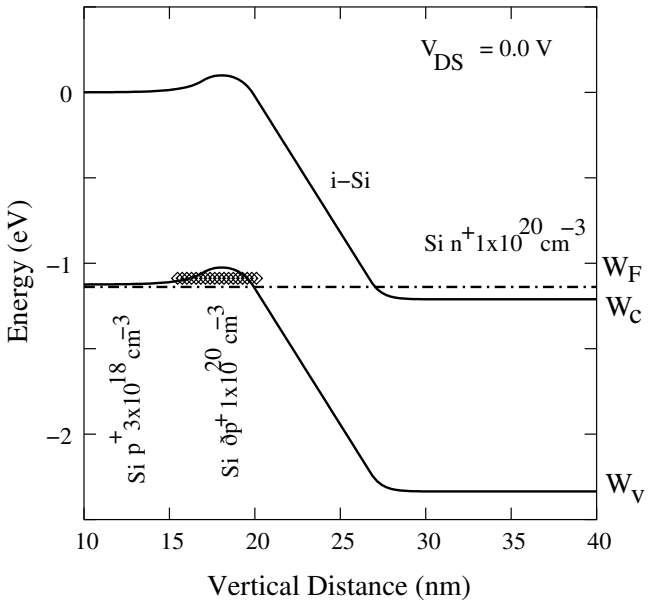

Figure 3.17: *1-D quantum mechanical simulated (NEMO) bands for the Si tunnel FET (only the p-i-n diode is simulated) with a δp^+ layer. The simulated resonant state is shown.*

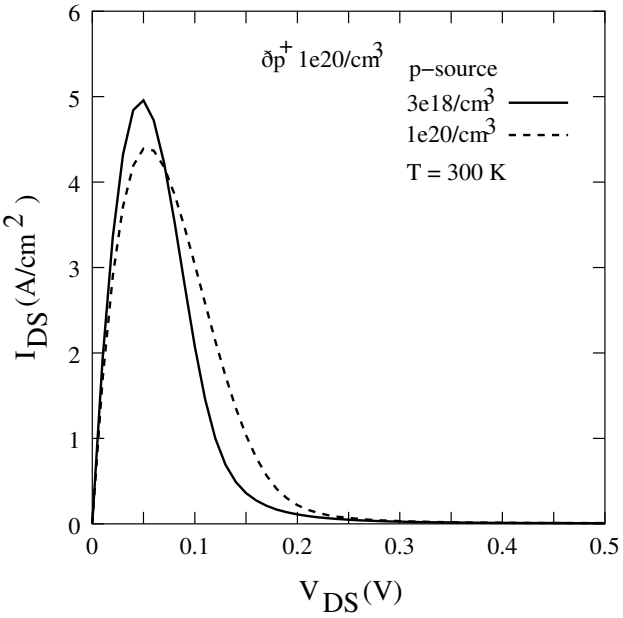

Figure 3.18: *1-D simulated $I-V$ curve of the p-i-n diode with change in source doping. As can be seen, source doping has little effect on the current density as well as peak voltage, V_p.*

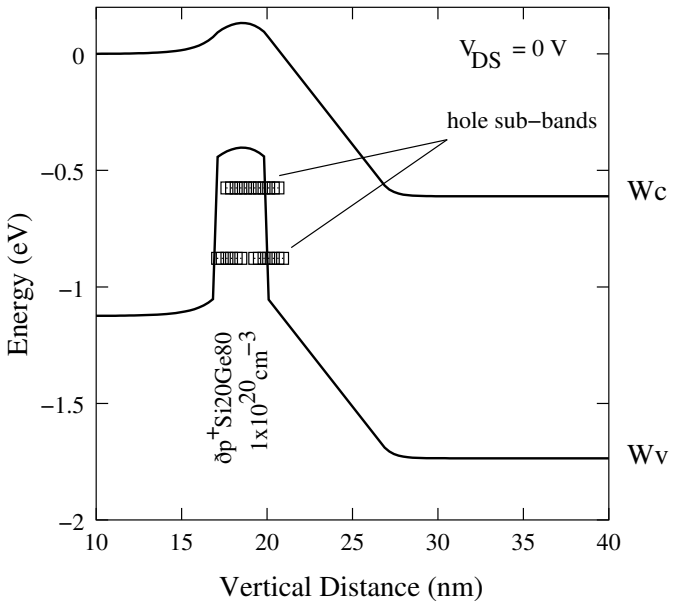

Figure 3.19: *1-D simulated bands for the heterosturcture SiGe tunnel FET (only the p-i-n diode is simulated). Ge content, x, is chosen to be 0.8 with a constant effective mass of silicon. Multiple resonant states, corresponding to hole sub-bands are observed.*

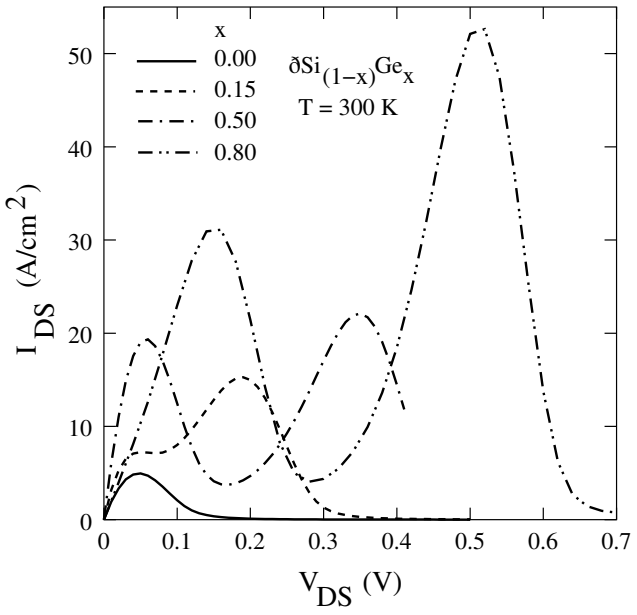

Figure 3.20: *1-D simulated $I-V$ curves for the heterostructure p-i-n diode corresponding to Fig. 3.19. Multiple peaks are observed. Further, the peak current density increases with increasing Ge content, x.*

that can be achieved within reasonable operating voltages. Recalling Eq. 1.8 for a conventional MOSFET I_{off},

$$I_{off} = I_{VT} 10^{-V_T/S}, \tag{3.12}$$

for constant S, I_{off} is limited by the V_T value. However, since S for a tunnel FET is decaying rapidly with lowering V_{GS}, the current falls off faster than exponential. Further, for the tunnel FETs, the lower limit of I_{off} is determined by the I_{bulk} value. This leads to the possibility of optimizing the tunnel FETs to achieve a lower I_{off} at lower V_T values even as the devices are scaled down. The scaling issues of the tunnel FET will be discussed in the following chapter.

Chapter 4

Scaling Issues of Tunnel FETs

In this chapter, scaling issues of the tunnel FETs are presented. The scaling parameters of Si homogeneous tunnel FET are subjected to the conventional MOSFET scaling rules as discussed in chapter 1. In chapter 2, it was shown that the tunnel FET transfer characteristics can be described by one equation for both the on- as well as the off-region of operation. Thus, the tunnel FETs follow different scaling rules in comparison to the conventional MOSFETs. Since scaling both L and t_{ox} does not improve the tunnel FET performance, it is shown that SiGe provides and additional scaling parameter in addition to both L and t_{ox}. Further, improvements with SiGe are significantly higher than with t_{ox} scaling alone. This is further advantageous as the tunnel FETs can be scaled without the need of scaling t_{ox} aggressively. However, with increasing Ge content, x, in SiGe, I_{off} starts to increase rapidly as tunneling probability becomes significant even at $V_{GS} = 0$ V. Engineering the gate workfunction by proper choice of gate material can significantly lower I_{off} to the bulk p-i-n diode current, I_{bulk}. Thus, the optimization of the tunnel FETs to achieve high I_{on}/I_{off} current ratio is then done by appropriate choice of Ge content, x, gate oxide thickness, t_{ox}, and gate-workfunction, ϕ_m.

4.1 ITRS Requirements

As the lateral dimensions L and W of the conventional MOSFET are scaled in order to squeeze in more devices on the same chip, t_{ox} and other vertical dimensions are also scaled in order to keep the short-channel effects under control. This, however, leads to several undesirable effects in the device performance, as discussed in chapter 1, and scaling becomes more and more challenging. Before discussing the effects of scaling the geometry parameters on the tunnel FET performance, a review of some of the electrical parameter requirements, like I_{on}, I_{off} and V_T, as predicted by the ITRS [68] for future CMOS technologies, is done for both the high performance logic and low power applications.

Table 4.1 lists the *near term* (2003-2009) electrical parameter requirements. While a higher saturation drive current is needed for high performance logic, a lower leakage current is needed for low operating power.

Table 4.1: *ITRS requirements for high performance logic and low operating power.*

High Performance Logic:	*Near-Term (2003-2009)*
L	45 - 20 nm
I_{on}	980 - 1590 μA/μm
V_T	0.21 - 0.16 V
I_{off}	0.03 - 0.07 μA/μm
V_{DD}	1.2 - 1.0 V
Low Operating Power:	*Near-Term (2003-2009)*
L	65 - 25 nm
I_{on}	520 - 770 μA/μm
V_T	0.31 - 0.25 V
I_{off}	1 - 5 pA/μm
V_{DD}	1.0 - 0.8 V

4.2 Scaling the Si Homogeneous Tunnel FET

Scaling properties of the Si homogeneous tunnel FET as discussed in chapter 2 are briefly reviewed. First, a discussion of the effects of channel doping, N_i, on the tunnel FET performance is done followed by the scaling of t_{ox} and L. Since the tunnel FETs follow different scaling rules, strict ITRS guidelines are not followed here in determining these parameters. Instead a general discussion is made for L and t_{ox} scaling. As the effect of p^+ source doping profile and smear-out effects on the n-channel tunnel FET electrical parameters like I_{on} and V_T has been discussed in detail in [85, 89], these are not discussed here. Thus, as discussed in chapter 2, optimum and technologically relevant doping profiles at the p^+ source and n^+ drain regions as $N = 1{\times}10^{20}\text{cm}^{-3}$ is chosen.

4.2.1 Channel Doping, N_i

The channel doping, N_i, is kept at the unintentional MBE growth doping impurity level of $1{\times}10^{15}\text{cm}^{-3}$ n-type. For conventional MOSFETs, the substrate doping, N_a, is increased by the scaling factor, α, to achieve the desired V_T and keep the short channel effects under control. However, for the tunnel FETs it is desirable to have the channel intrinsic or lightly doped. The tunnel FET V_T is determined by E_{max} across the tunnel junction and is not directly controlled by N_i. Further, for low channel doping level $N_i << N$, E_{max} is only weakly dependent on N_i. This can be seen from Eqs. A.22 (see Appendix A)

$$E_{max-p\pi n} = \frac{qN}{\epsilon_s}(x_n + \frac{N_i}{N}L) \tag{4.1}$$

and A.25

$$E_{max-pin} = \frac{qN}{\epsilon_s}x_n \approx \frac{\psi_0}{L} \tag{4.2}$$

where x_n is the depletion width in the source region and ψ_o is the built-in potential of the p-i-n diode. Thus, for large values of $N_i \approx N$, $E_{max-p\pi n}$ starts to increase with increase in N_i. The junction leakage current in the absence of the gate bias (I_{DS} at $V_{GS} = 0$ V) then starts

to increase resulting in an increase in I_{off}. Further, the increase in I_{on} is not as significant as the increase in I_{off} due to the strong dependence of swing S on V_{GS}. Furthermore, since $L >> x_n$, the increase in $E_{max-p\pi n}$ and hence I_{DS} is insignificant. Therefore an increase in N_i for tunnel FETs is not desirable as an undoped channel also avoids problems related to the statistical fluctuation of dopant atoms in the channel (section 1.1.3).

4.2.2 Channel Length, L

Since direct tunneling between source and drain for $V_{GS} = 0$ V can be neglected for channel lengths above 10 nm in silicon, the tunnel FETs show a nearly L independent transfer characteristics. Fig. 4.1 shows the transfer characteristics of a n-channel silicon tunnel FET as a function of L at $V_{DS} = 1.0$ V. L is scaled from 100 nm to 25 nm at constant $t_{ox} = 2$ nm. As expected, it is observed that the on-current, I_{on}, and threshold voltage, V_T, are nearly independent of L scaling. I_{off}, on the other hand, remains at ≈ 1 fA/μm corresponding to the reverse biased p-i-n diode diffusion current, for L scaling from 100 nm to 32 nm. As L is further scaled to 25 nm, a sharp exponential increase in I_{off} is seen. This happens as the p-i-n diode Zener breakdown limit is reached. Thus, in order to control the p-i-n diode Zener breakdown, it would be necessary to scale the supply voltage, V_{DD}. However, even under these conditions, I_{off} observed is less than 1 pA/μm which is well below the technology requirements for both the high performance logic as well as low operating power.

For a conventional MOSFET, I_{DS} increases with lowering in L (Eqs. 1.4 and 1.6) resulting in an increase in both I_{off} and I_{on}. The L invariant transfer characteristics of the tunnel FET though, has an advantage over the conventional MOSFETs. Statistical variations in L lead to V_T variations in conventional MOSFETs on the same wafer. This effect becomes more stringent as the devices are scaled down. This is absent for the tunnel FETs. Further, with L scaling, SCE like V_T rolloff is absent in tunnel FETs.

4.2.3 Oxide Thickness, t_{ox}

In this sub-section, the effect of oxide thickness scaling on the tunnel FET performance is investigated. Fig. 4.2 shows the transfer characteristics for a 100 nm n-channel tunnel FET as a function of t_{ox} which is scaled from 4 nm to 1 nm at $V_{DS} = 1.0$ V. In order to compare the different devices, the maximum applied V_{GS} for each t_{ox} is chosen to have a maximum potential drop of 1 V/nm across the oxide. That is, at constant maximum electric field, E_{ox}, across the oxide.

As can be seen from Fig. 4.2, I_{off} increases for $t_{ox} = 1$ nm as the tunneling currents start to dominate at $V_{GS} = 0$ V. While I_{off} remains at the I_{bulk} value for t_{ox} scaling from 4 nm to 2 nm, I_{b2b} starts to dominate for $t_{ox} < 2$ nm. Thereby, increasing I_{off}. However, it still remains several orders of magnitude below the ITRS requirements. It should be further noted that the best achievable value of I_{off} is determined by the bulk p-i-n diode leakage current, I_{bulk}, which is independent of t_{ox}. This can be achieved by appropriate gate work-function engineering which will be discussed in detail later in the chapter. However, with t_{ox} scaling, the tunneling leakage current through thin oxides (both direct tunneling as well as Fowler-Nordheim tunneling) as discussed in section 1.1.2, will limit the I_{off}.

I_{on}, on the other hand, decreases with decreasing t_{ox} as the maximum applied V_{GS} is scaled proportionately. This is due to the fact that V_T is not scaled as much as the maximum V_{GS} for each t_{ox}. This is shown in Fig. 4.3. V_T lowers from 1.72 V for $t_{ox} = 4$ nm to 0.425

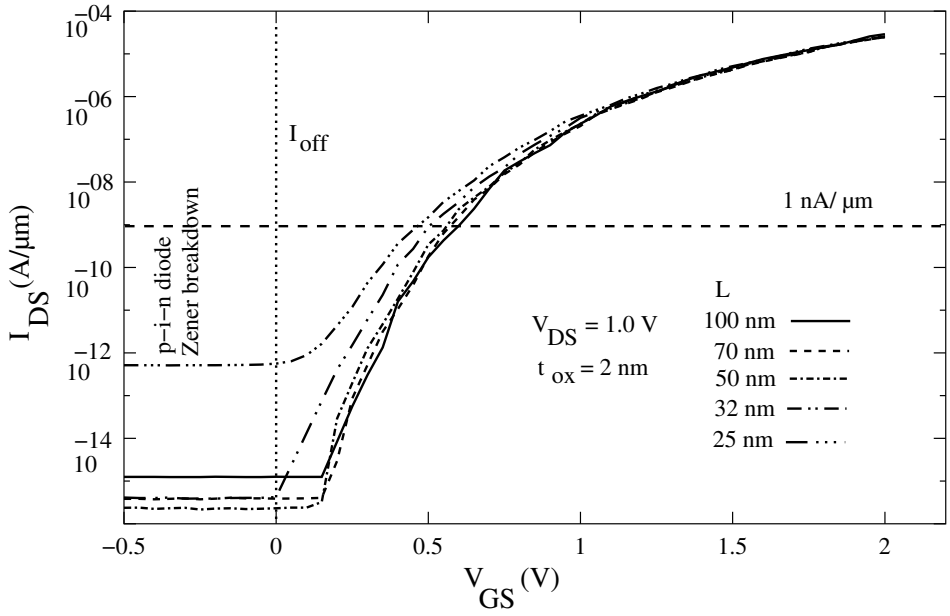

Figure 4.1: *N-channel Si tunnel FET transfer characteristics for L scaling from 100 nm to 25 nm ($t_{ox} = 2$ nm). I_{on} and V_T remain independent of L while I_{off} increases exponentially for $L = 25$ nm as the p-i-n diode Zener breakdown limit is reached.*

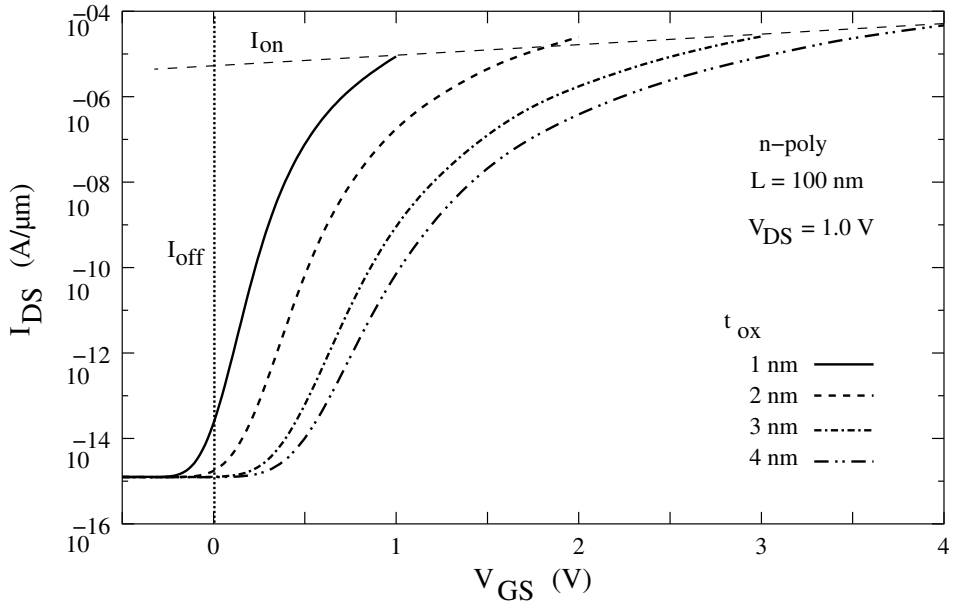

Figure 4.2: *N-channel transfer characteristics for a 100 nm Si tunnel FET as a function of t_{ox} at $V_{DS} = 1$ V. I_{on} is seen to degrade while I_{off} starts to increase for $t_{ox} < 2$ nm.*

for t_{ox} = 0.8 nm. Further, for L = 100 nm and t_{ox} = 2 nm, I_{on} achieved is $\approx$ 10 μA/μm at a V_T of nearly 1 V. This is well below the technology requirements of I_{on} of 1000 μA/μm at a V_T of 0.2 V. Since V_T does not directly depend on the channel inversion charge, but is determined by the tunneling probability as a result of the formation of the p^+n^+ tunnel junction, it not a strong function of t_{ox}. Thus, there is an overall degradation in I_{on}, and I_{on}/I_{off} ratio lowers with scaling t_{ox}.

The effective subthreshold swing S for tunnel FETs is seen to improve with decreasing t_{ox} (Fig. 4.4). Thus, improving the turn-on performance. While S for I_{DS} increasing from I_{bulk} at $V_{GS} = V_{off}$ to I_{VT} at $V_{GS} = V_T$, is 100 mV/dec for a t_{ox} of 2 nm, it reduces to 57 mV/dec for a t_{ox} of 0.8 nm. Thus, as predicted in section 3.3.3, it is observed that the effective S can be less than 60 mV/dec at room temperatures even for the Si tunnel FETs.

I_{on} is independent of L scaling but degrades with t_{ox} scaling. Since L must be scaled for faster performance and higher density of devices on the chip, t_{ox} must also be scaled in order to achieve a stronger gate control. This is illustrated in figures 4.5 and 4.6 where output characteristics for the Si tunnel FET is shown with t_{ox} = 4 nm and 1 nm, respectively. For a thinner gate oxide material, a stronger gate control results in a much better short-channel performance and hence the saturation behavior. It is also seen from the figures that while I_{on} for t_{ox} = 4 nm at V_{DS} = 2 V is nearly 40 μA/μm, the saturation drive current drops to 4.5 μA/μm for t_{ox} = 1 nm resulting in degraded performance as discussed above.

Thus, apart from channel length, L, source and channel dopingi, N_A and N_i, respectively, and oxide thickness, t_{ox}, there is need for another parameter to both allow scaling and improve the tunnel FET performance.

4.3 Scaling the Tunnel FET with δp^+ SiGe Layer

As discussed in chapter 3, the performance of the n-channel tunnel FETs can be significantly enhanced with bandgap modulation, in this section, the scaling issues with the δp^+ SiGe layer is investigated. Along with incorporation of SiGe, L and t_{ox} are scaled simultaneously. It is shown that with L scaling, the p-i-n diode Zener breakdown is reached earlier for a heterojunction SiGe tunnel FET than for the Si homogeneous tunnel FET. Since L here is scaled from 100 nm to 50 nm, within the p-i-n diode Zener breakdown limit, the change in both I_{on} and I_{off} is negligible with L scaling. At the p-i-n diode breakdown limit, only I_{off} is affected which start to increase exponentially. V_T and I_{on} however, remain unchanged. Further, the performance improvement with the Ge content, x increasing is much significant than that for t_{ox} scaling.

In Fig. 4.7 the n-channel transfer characteristics for the tunnel FET with the δp^+ SiGe layer at the p-source end for L =100 nm and t_{ox} = 2 nm (Fig. 3.7 reproduced here) is shown. As has been discussed in chapter 3, I_{on} and V_T are seen to improve considerably with increasing Ge content, x. Beyond x = 0.3, I_{off} increases exponentially as I_{b2b} at V_{GS} = 0 V starts to increase and becomes more dominant. It is further observed that application of a small negative V_{GS} lowers I_{off} significantly. This happens as the bands are pulled apart and thereby lower the tunneling probability. Thus, for L = 100 nm, t_{ox} = 2 nm and Ge content x = 0.5, I_{on} = 900 μA/μm. I_{off} on the other hand, rises 5 orders of magnitude to 300 pA/μm. Since this is still below the ITRS requirements for both the high speed and low operating power, it does not pose a serious problem.

As t_{ox} is scaled along with L to maintain good saturation behavior, I_{off} further rises due

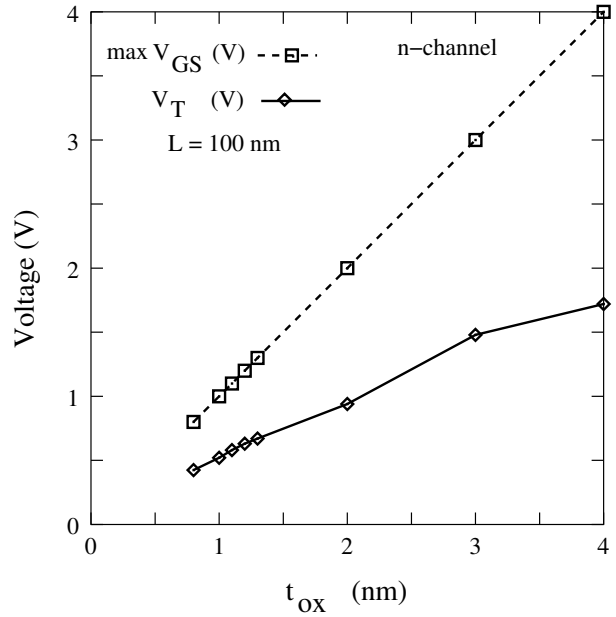

Figure 4.3: *N-channel V_T variation with t_{ox} scaling. In order to keep E_{ox} constant, maximum V_{GS} applied across the oxide is scaled. As V_T does not scale as much as maximum V_{GS}, it results in degraded performance.*

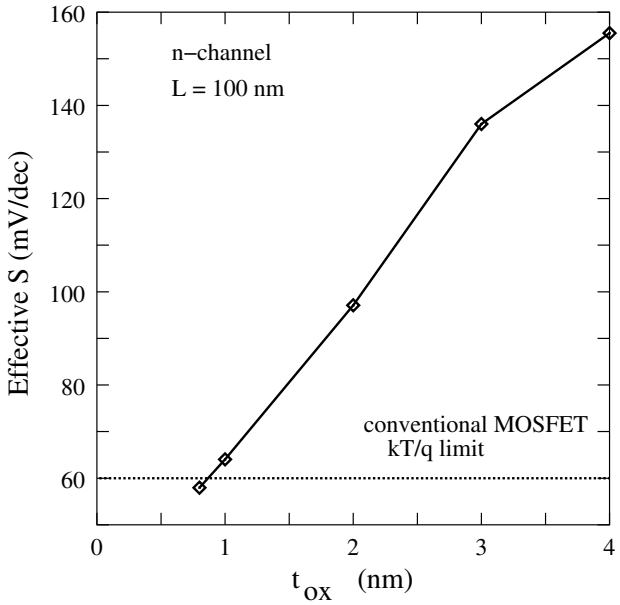

Figure 4.4: *Effective subthreshold swing, S for a Si tunnel FET as a function of t_{ox} (L = 100 nm). S can be less than 60 mV/dec even at T = 300 K.*

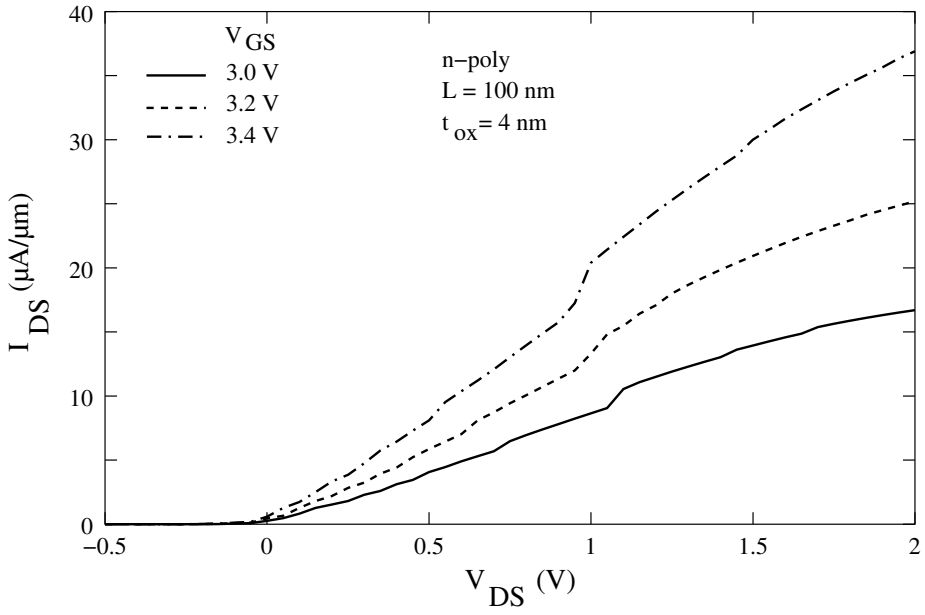

Figure 4.5: *N-channel output characteristics for $L = 100$ nm and $t_{ox} = 4$ nm Si tunnel FET. The device does not show saturation behavior due to poor gate control.*

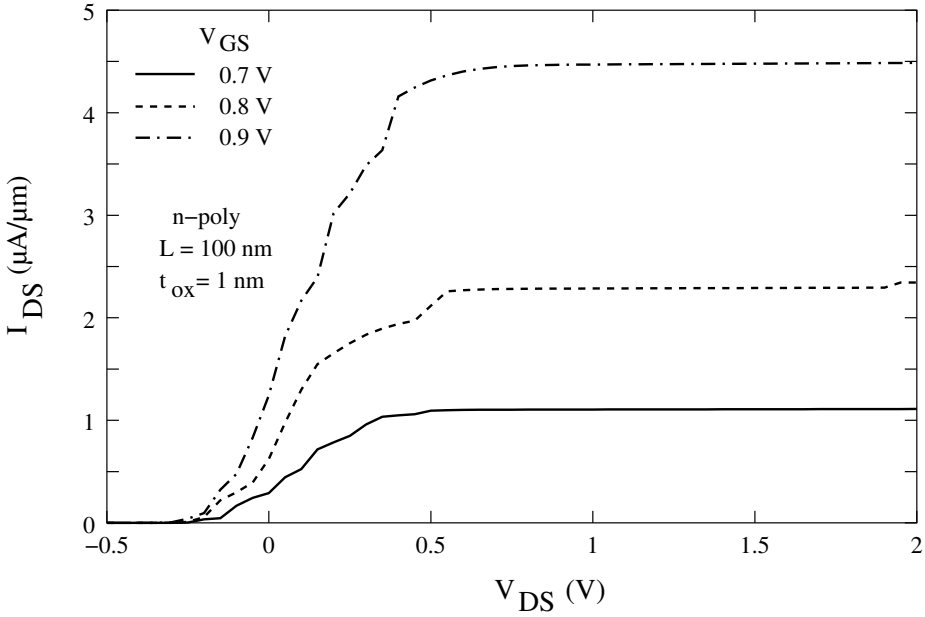

Figure 4.6: *N-channel output characteristics for $L = 100$ nm and $t_{ox} = 1$ nm Si tunnel FET. Excellent saturation behavior is achieved due to a strong gate control.*

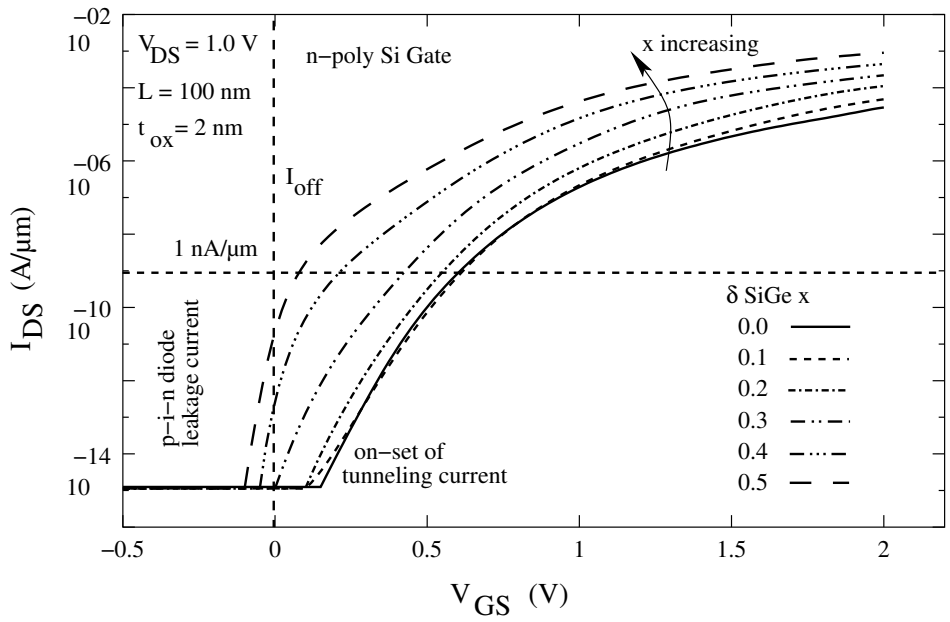

Figure 4.7: *N-channel transfer characteristics for $L = 100$ nm and $t_{ox} = 2$ nm tunnel FET as a function of Ge content, x.*

to a lowering of V_T. This is shown in Fig. 4.8 which shows the transfer characteristics for the heterogeneous SiGe tunnel FET with $L = 70$ nm and $t_{ox} = 1.5$ nm. I_{on} for each x is *lowered* and I_{off} increases. For Ge content $x = 0.5$, I_{on} of 895 μA/μm and I_{off} of 1.6 nA/μm is achieved. Thus, while there is marginal loss in I_{on}, I_{off} has risen by another factor of 5. Though I_{off} is good enough for high speed applications, it is not desirable for low operating power.

The effect becomes more pronounced for $L = 50$ nm and $t_{ox} = 1.2$ nm (Fig. 4.9). In this case, increase in I_{b2b} at $V_{GS} = 0$ V raises I_{off} to 5 nA/μm for $x = 0.5$, which becomes unacceptable even for high performance logic. I_{bulk} is also seen to increase considerably as the p-i-n diode Zener breakdown (V_Z) limit is reached. Thus, while the Si homogeneous tunnel FET can be scaled to below 30 nm before the p-i-n diode Zener breakdown limit is reached, the SiGe tunnel FET V_Z is reached as early as $L = 50$ nm. Since I_{bulk} starts to increase exponentially with L scaling, this becomes a limiting factor in determining I_{off}. I_{on} is seen to decrease by another 30% to 660 μA/μm.

Figures 4.10 and 4.11 show the output characteristics for the two technology nodes for $L = 70$ nm and 50 nm respectively. Scaling t_{ox} to 1.5 nm and 1.2 nm results in better gate control and the scaled tunnel FETs show similar saturation behavior.

Fig. 4.12 shows the n-channel V_T as a function of increasing Ge content, x, increasing and t_{ox} scaling. For the Si tunnel FET ($x = 0$), V_T is lowered from 0.90 V to 0.66 V (about 27%) for t_{ox} scaling from 2.0 nm to 1.2 nm as L is scaled from 100 nm to 50 nm. Thus, for each L and t_{ox}, the Si tunnel FET V_T is higher than the ITRS requirements. Further, with decreasing t_{ox}, the probability of direct tunneling through oxide is increasing exponentially (see for eg. [29]), resulting in a significant increase in the undesirable gate tunneling leakage currents.

However, as the Ge content, x, is increased in the heterojunction SiGe tunnel FET, a

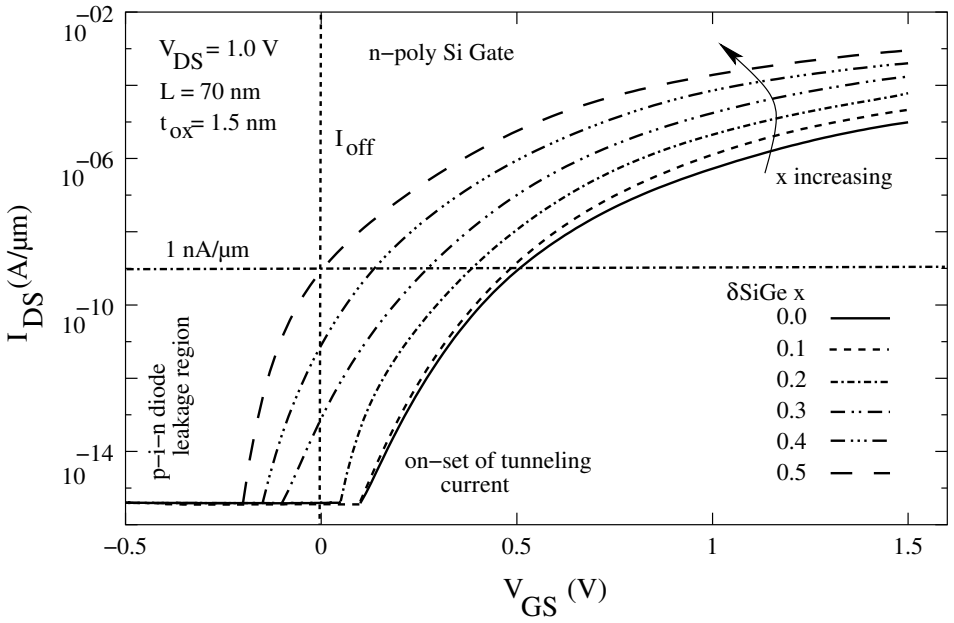

Figure 4.8: *Input characteristics for a 70 nm channel length n-channel tunnel FET as a function of x.*

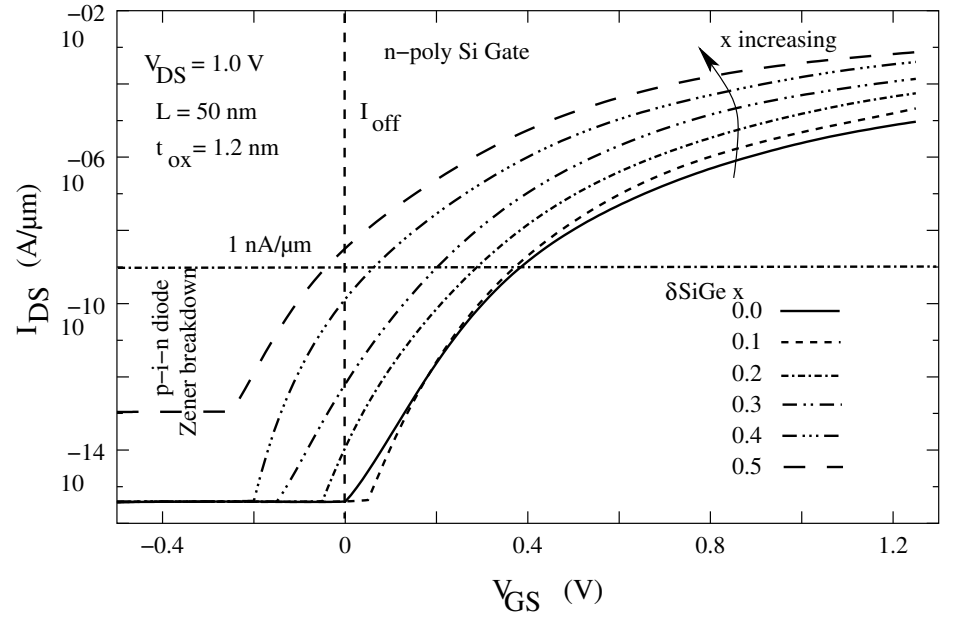

Figure 4.9: *Input characteristics of a $L = 50$ and $t_{ox} = 1.2$ nm n-channel tunnel FET as a function of Ge content x.*

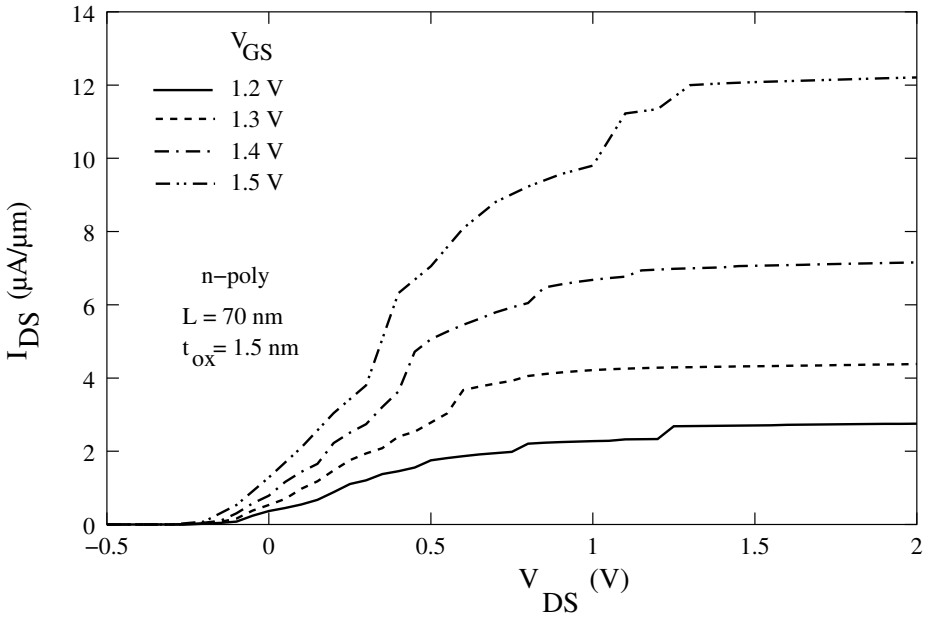

Figure 4.10: *Output characteristics of a $L = 70$ nm and $t_{ox} = 1.5$ nm n-channel Si tunnel FET. Good saturation behavior is observed.*

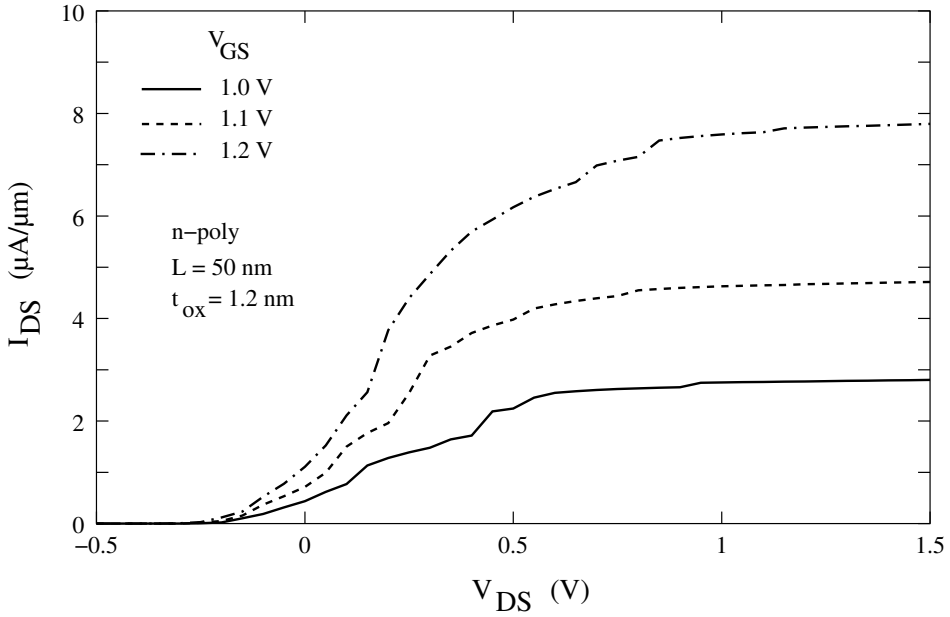

Figure 4.11: *Output characteristics of a $L = 50$ nm and $t_{ox} = 1.2$ nm n-channel Si homogeneous tunnel FET.*

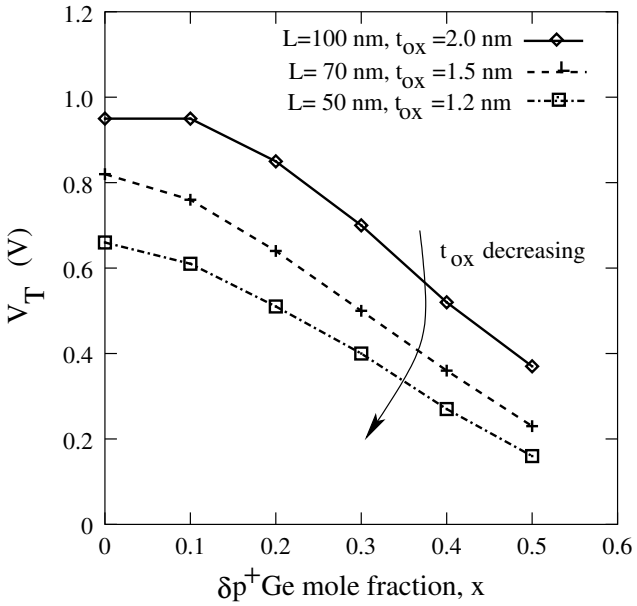

Figure 4.12: *V_T as a function of x for L = 100-, 70-, and 50 nm with t_{ox} = 2.0-, 1.5-, and 1.2 nm.*

significant lowering in V_T as a function of x is seen. Thus, for x increasing from 0.0 to 0.5, the V_T lowers from 0.90 V to 0.30 V (almost 70%) for $L = 100$ nm and $t_{ox} = 2$ nm; from 0.82 V to 0.23 V (almost 72%) for $L = 70$ nm and $t_{ox} = 1.5$ nm; and, from 0.66 V to 0.16 V (almost 75%) for $L = 50$ nm and $t_{ox} = 1.2$ nm. Thus, it is observed that the Ge content, x, plays a dominating role in determining the tunnel FET parameters than the oxide thickness, t_{ox}, and channel length, L.

Further, as shown in Fig. 4.13, increase in x also leads to a lowering in the effective subthreshold swing, S, for each technology node and can be less than 60 mV/dec at room temperature. While, as discussed in section 4.2, a sub-60 mV/dec effective room temperature swing is achieved for a $t_{ox} < 0.8$ nm for the silicon tunnel FET with SiGe it can be achieved for even thicker t_{ox}. Thus, effective S lowers from 96 mV/dec to 54 mV/dec for x increasing from 0 to 0.5 for $L = 100$ nm and $t_{ox} = 2$ nm. For a thinner t_{ox}, it is lowered even further. Thereby, allowing the possibility of scaling the tunnel FETs with improved I_{on}/I_{off} ratios even as the devices are scaled down.

Fig. 4.14 shows the band-to-band tunneling generation rate G_{b2b} as a function of x and t_{ox} scaling. It is clearly seen that x is the dominating parameter in comparison to both L and t_{ox} scaling. Thus, while G_{b2b} increases only 8 orders of magnitude for t_{ox} scaling from 2.0 nm to 1.2 nm for the Si tunnel FET ($x = 0$), it increases by a mammoth 17 orders of magnitude for x increasing from 0 to 0.5 for $t_{ox} = 2$ nm. Similar gain is observed for t_{ox} of 1.5 nm and 1.2 nm where G_{b2b} increases by 15 and 12 orders of magnitude respectively. Further, as x increases, performance improvement with t_{ox} scaling is only marginal as can be seen from the increase in G_{b2b} for $x = 0.5$, which less than 2 orders of magnitude. This happens as the tunnel junction field, E_{max}, is controlled more by the p-source region and less by the charge in the channel. Thus, as discussed in section 3.2 (Fig. 3.5), as x increases, G_{b2b} increases sharply even for $V_{GS} = 0$ V. This results in a high tunneling probability and exponentially increasing leakage current, I_{off}.

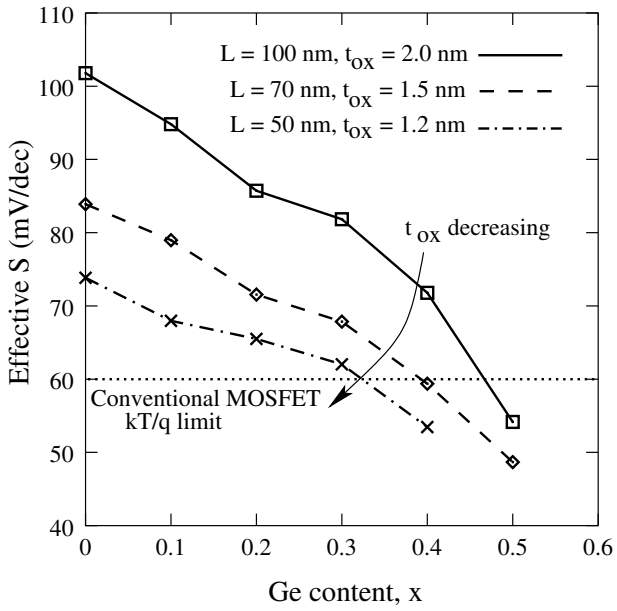

Figure 4.13: *Effective subthreshold swing S as a function of Ge content x for L=100-, 70-, and 50 nm and t_{ox} = 2.0-, 1.5- and 1.2 nm. Improvement in S with x is much more significant than that with t_{ox} scaling.*

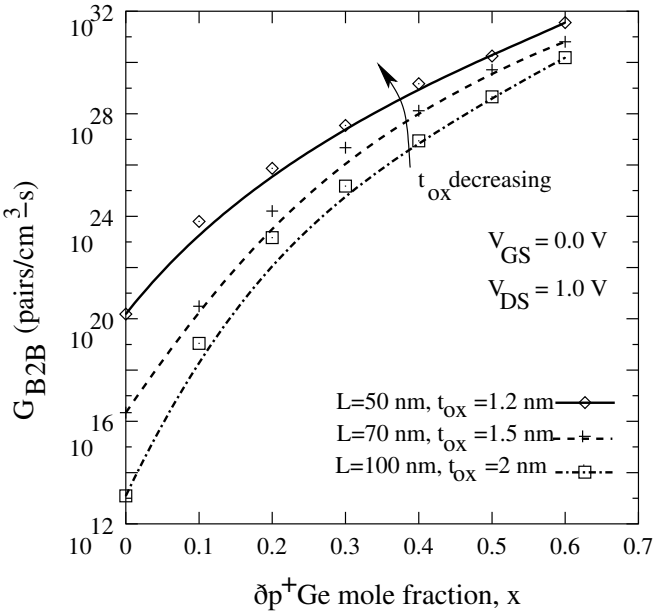

Figure 4.14: *G_{b2b} as a function of x for L = 100-, 70-, and 50 nm with t_{ox} = 2.0-, 1.5-, and 1.2 nm. Increase in G_{b2b} is much more significant with x increasing than with t_{ox} scaling.*

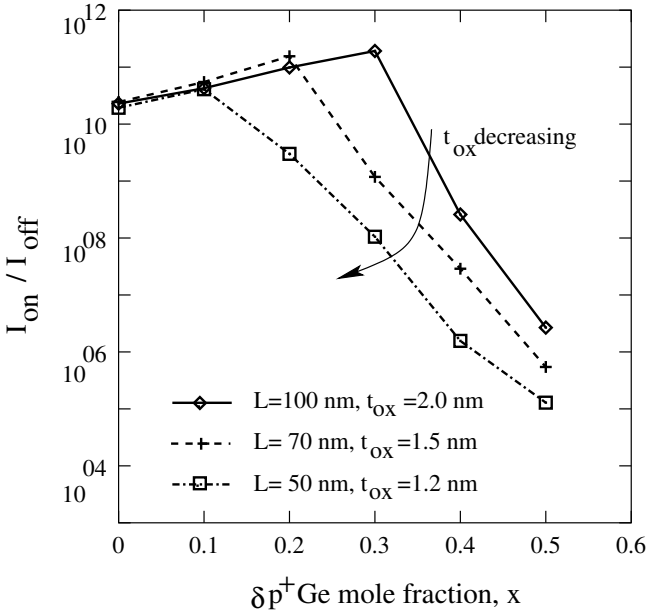

Figure 4.15: *I_{on}/I_{off} as a function of x for L = 100-, 70-, and 50 nm and t_{ox} = 2.0-, 1.5-, and 1.2 nm.*

Fig. 4.15 shows the I_{on}/I_{off} ratio for the tunnel FET with SiGe and L and t_{ox} scaling. For the Si tunnel FET ($x = 0$), a *nearly* constant and already a very high I_{on}/I_{off} of 10^{10} is achieved for all value of t_{ox} and L. This is already 4-5 orders of magnitude higher than that achieved for close to the ideal conventional MOSFETs. While I_{off} remains constant at I_{bulk}, there is slight lowering in I_{on} as t_{ox} is scaled. As the Ge content, x, increases for the heterojunction SiGe tunnel FET, I_{on}/I_{off} ratio increases as long as I_{off} remains constant and I_{on} increases. However, beyond the p-i-n diode Zener breakdown limit, I_{off} starts to increase exponentially, leading to a sharp drop in the I_{on}/I_{off} ratio. While I_{on} continues to increase with increase in x, the improvement is negligible in comparison to the degradation in I_{off}. This is due to the fact that 'spot' S for tunnel FETs is a strong function of V_{GS} and is degrading with increase in V_{GS}. Thus, I_{DS} at $V_{GS} = 0$ V (I_{off}) increases faster than I_{DS} at $V_{GS} = V_{DD}$ (I_{on}).

The effect becomes more pronounced due to a lowering in V_T and improving S as t_{ox} is scaled. Thus, while the I_{on}/I_{off} ratio starts to fall beyond $x = 0.3$ for $t_{ox} = 2$ nm, it starts to lower beyond $x = 0.2$ for $t_{ox} = 1.5$ nm and beyond $x = 0.1$ for $t_{ox} = 1.2$ nm. This is demonstrated in terms of the technology requirements in Fig. 4.16 which shows the *normalized* I_{off} versus *normalized* I_{on} as the tunnel FET is scaled with x increasing. Thus, for x beyond 0.3, while I_{on} increases to meet the ITRS requirement for low operating power for all values of L and t_{ox}, I_{off} remains below the 1 nA/μm requirement. For $t_{ox} = 1.2$ nm, and $x = 0.5$, I_{off} exceeds the 1 nA/μm limit due to the p-i-n diode Zener breakdown as can also be seen from Fig. 4.9. The results are summarized in Table 4.2 which lists the tunnel FET electrical parameters with change in L, t_{ox} and Ge content, x. Fig. 4.17 is the 3-D plot of I_{on} as a function of t_{ox} and Ge content, x. Thus the choice of x and t_{ox} can be made for any required I_{on} and I_{off} for a desired channel length, L.

Thus, in general, the heterojunction SiGe tunnel FET meets the ITRS requirements

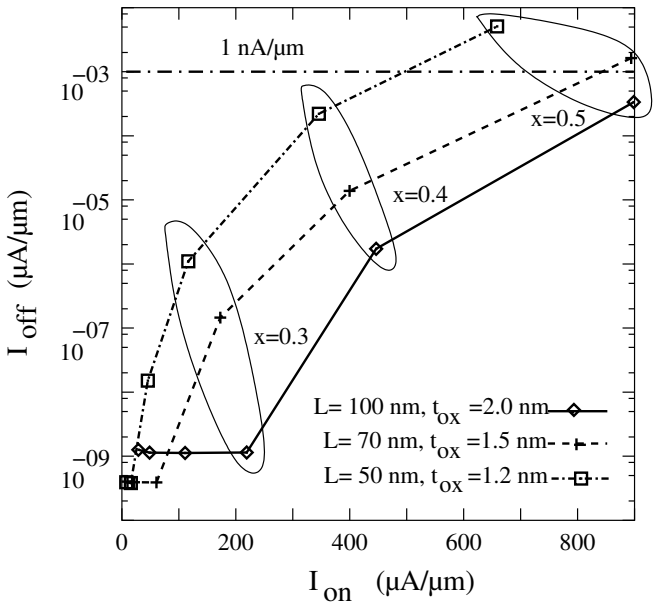

Figure 4.16: *Normalized I_{on} versus I_{off} as a function of x for L = 100-, 70-, and 50 nm with t_{ox} = 2.0-, 1.5-, and 1.2 nm.*

Table 4.2: *Tunnel FET parameters as a function of L, t_{ox} and Ge content, x*

L (nm)	t_{ox} (nm)	x	I_{on} (μA/μm)	I_{off} (μA/μm)	V_T (V)	S (mV/dec)
100	2.0	0.0	28.9	1.26×10^{-09}	0.90	96
100	2.0	0.1	48.5	1.14×10^{-09}	0.85	89
100	2.0	0.2	111.1	1.12×10^{-09}	0.72	84
100	2.0	0.3	219.2	1.14×10^{-09}	0.56	72
100	2.0	0.4	446.2	1.73×10^{-06}	0.41	66
100	2.0	0.5	898.6	3.36×10^{-04}	0.29	54
70	1.5	0.0	12.2	0.40×10^{-09}	0.82	84
70	1.5	0.1	21.4	0.39×10^{-09}	0.76	79
70	1.5	0.2	60.7	0.39×10^{-09}	0.64	72
70	1.5	0.3	172.8	1.46×10^{-07}	0.49	68
70	1.5	0.4	399.7	1.38×10^{-05}	0.36	59
70	1.5	0.5	894.1	1.64×10^{-03}	0.23	48
50	1.2	0.0	7.6	0.39×10^{-09}	0.66	74
50	1.2	0.1	15.7	0.38×10^{-09}	0.61	68
50	1.2	0.2	45.5	15.1×10^{-09}	0.51	65
50	1.2	0.3	116.5	1.11×10^{-06}	0.40	62
50	1.2	0.4	345.8	2.22×10^{-04}	0.27	54
50	1.2	0.5	658.8	5.11×10^{-03}	0.16	-

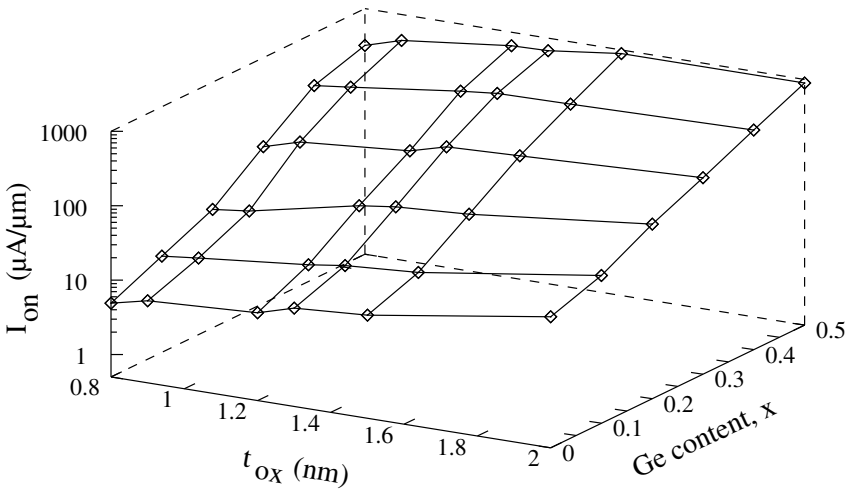

Figure 4.17: *3-D plot showing the dependence of I_{on} on t_{ox} and Ge content, x.*

for both high performance and low operating power in terms of I_{on}. I_{off} however, increases beyond the low operating power requirements. In the following a possible solution is suggested to overcome the high off-current in order to achieve a high I_{on} at the same time maintaining low leakage currents.

4.4 Gate Workfunction Engineering

The minimum value of I_{off} that can be achieved for tunnel FETs is the reverse biased p-i-n diode diffusion leakage current, I_{bulk}. I_{bulk} in general is *independent* of t_{ox} and gate material and parameters like workfunction, ϕ_m, and doping, but strongly depends on source, drain and channel doping profiles, L and mesa width, W.

As it has been shown in figures 4.7, 4.8 and 4.9, the tunnel FET I_{off} starts to increase with increasing Ge content, x. However, application of a small negative gate voltage leads to a sharp drop in the drain current. This is due to the fact that when a negative V_{GS} is applied, the bands are pulled apart leading to a sharp drop in the tunneling probability, and hence the tunneling current. This results in *orders of magnitude* lower leakage currents.

An alternative technological way to obtain the same result is to do a gate workfunction engineering so as to shift the curves in order to get a higher V_T in proportion to workfunction shift, $\Delta\phi_m$. This, as discussed in section 1.1 will also result in an increase in V_T by $\Delta\phi_m$. Since I_{on} for tunnel FETs is calculated at a constant *maximum* potential drop of 1 V/nm across the gate-oxide, the increase in V_T will result in a *loss* in I_{on}. However, as the tunnel FET swing is independent of ϕ_m but degrades with increase in V_{GS}, I_{DS} is falling much faster below $V_{GS} = V_T$, when the tunnel FET is off, than for $V_{GS} > V_T$ values when it is on. This results in only a marginal loss in I_{on}. Thus, there is a *significant* overall improvement in the tunnel FET performance with gate workfunction engineering in term of I_{on}/I_{off} ratio.

Fig. 4.18 the n-channel transfer characteristics for a 32 nm channel length tunnel FET is shown. The device is chosen to illustrate the different parameters for gate workfunction engineering to improve the device performance. The t_{ox} and V_{DD} are scaled to 0.9 nm and 0.9 V respectively, and I_{on} is calculated at $V_{GS} = 0.9$ V. Since the bulk p-i-n diode is already

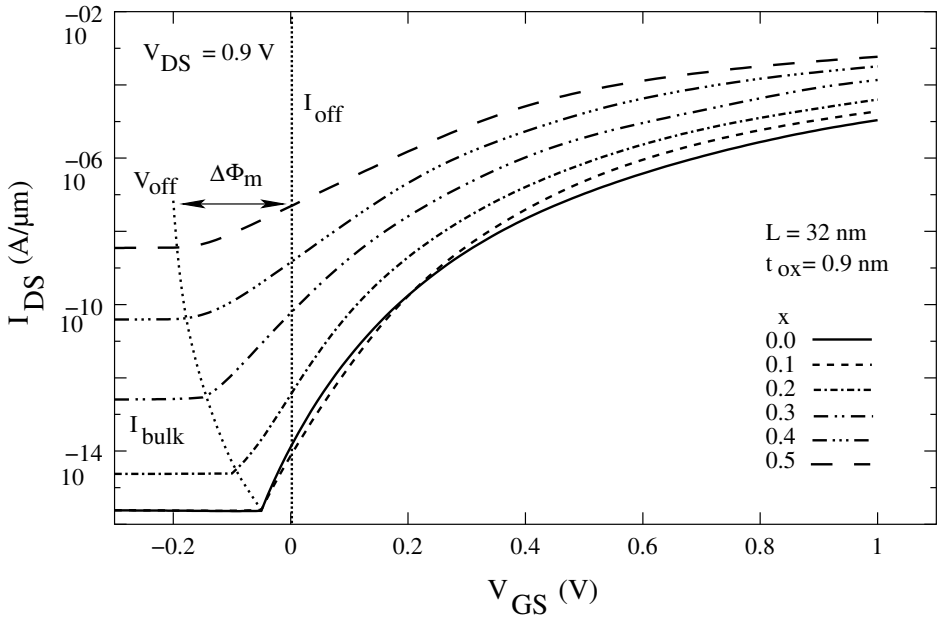

Figure 4.18: *N-channel transfer characteristics for tunnel FET for $L = 32$ nm and $t_{ox} = 0.9$ nm. As x increases, I_{bulk} increases exponentially due to the p-i-n diode Zener breakdown. V_{off} is lowered due to increased gate controlled tunneling probability.*

in the Zener breakdown ($V_{DS} > V_Z$) region for Ge content, $x > 0.1$, the device shows large *increasing* I_{bulk} with increase in x. Further, due to the thin t_{ox} even for $x < 0.1$, the tunnel FET has significant tunneling current at $V_{GS} = 0.0$ V due to a lower V_T. Optimization of this device in terms of I_{bulk} can be done by lowering the supply voltage, V_{DD} which would significantly lower I_{bulk}. This is because for $V_{DS} > V_Z$, I_{bulk} is falling exponentially with lowering in V_{DS}. Since in this section a discussion of I_{b2b} lowering with gate workfunction engineering is done, it is restricted to optimization in terms of I_{b2b}. Thus, for each x value, the I_{bulk} value can be achieved by *increasing* the V_T by changing the gate workfunction value, ϕ_m by $\Delta\phi_m$ as shown in the figure. Further, as can be seen from the $I_{DS} - V_{GS}$ characteristics of the heterostructure SiGe tunnel FETs in figures 4.7, 4.8 and 4.9, only a *small* V_T shift is needed to gain *largely* in I_{off}.

$\Delta\phi_m$ shifts of a few 100 mV have been reported with poly-SiGe gate electrodes [123–126] and workfunction tunable metal electrodes [127–129]. In metals, it is achieved by implantation of dopants into the silicon before silicidation process. During silicidation, it results in a high enough segregation of dopant concentration in a thin layer at the gate-dielectric interface so as to affect the composition in the gate material and hence the workfunction [130]. Thus, a higher than n^+ polysilicon and a lower than p^+ polysilicon workfunction has been reported.

Fig. 4.19 shows the simulated n-channel transfer characteristics of a 100 nm heterostructure SiGe tunnel FET with $t_{ox} = 2$ nm and Ge content $x = 0.4$ and 0.5. The device is similar to that of Fig. 4.7 except for the workfunction difference. N-polysilicon (constant $\phi_m = 4.1$ eV) was chosen as the gate material for all the values of x for the device in Fig. 4.7. This lead to an increase in I_{off} for $x = 0.4$ and 0.5. Since I_{off} for $x \leq 0.3$ is equal to I_{bulk}, no gate-workfunction engineering is needed for these values. However, as can be seen from Fig.

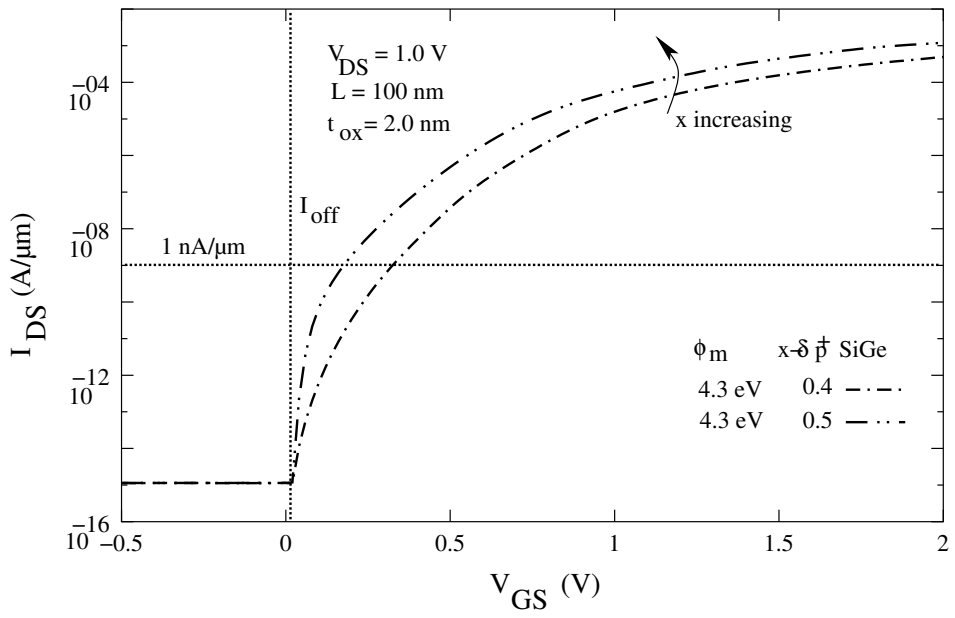

Figure 4.19: *N-channel transfer characteristics for tunnel FET with $x = 0.4$ and 0.5 ($L = 100$ nm, $t_{ox} = 2.0$ nm) with appropriate gate workfunction engineering.*

4.19, increasing ϕ_m by 0.2 eV for $x = 0.4$ and 0.5, leads to a lowering of I_{off} to the I_{bulk} value. Further, I_{on} still increases with increasing x implying that the loss in I_{on} is only marginal.

Fig. 4.20 shows the simulated n-channel transfer characteristics for a 70 nm channel length heterostructure SiGe tunnel FET with $t_{ox} = 1.5$ nm and for Ge content $x = 0.3$, 0.4 and 0.5 with ϕ_m shifts of 0.15 eV, 0.20 eV and 0.25 eV corresponding to ϕ_m of 4.25 eV, 4.30 eV and 4.35 eV, respectively. Similar computations are done for $L = 50$ nm and $t_{ox} = 1.2$ nm heterostructure SiGe tunnel FET with $\Delta\phi_m$ of 0.05 eV, 0.15 eV, 0.20 eV and 0.25 eV corresponding to ϕ_m of 4.15 eV, 4.25 eV, 4.3 eV and 4.35 eV for $x = 0.2$, 0.3, 0.4 and 0.5, respectively.

Thus, the corresponding *corrected* I_{on} values for *constant* I_{off} equivalent to I_{bulk} are shown in Fig. 4.21 for the three technology nodes considered here. Apart from lowering of I_{on} with t_{ox} scaling, it is observed that I_{on} increases for all values of x even after ϕ_m shifts for selected values of x which result in an increase in V_T. Thus, the loss in I_{on} for *each* x value after workfunction adjustment, is not significant and the tunnel FET performance improves. This is due to the fact that S is degrading with increasing V_{GS}.

The I_{on}/I_{off} ratio is shown in Fig. 4.22 with workfunction shifts. Unlike Fig. 4.15 where the I_{on}/I_{off} ratio initially increases and then falls exponentially, it is seen to increase here for all values of x. For $L = 50$ nm, $t_{ox} = 1.2$ nm and $x = 0.5$ it is seen to lower by more than 2 orders of magnitude as the p-i-n diode Zener breakdown limits I_{bulk}. Optimization of I_{bulk} can be done by scaling V_{DD} and mesa width, W.

4.5 Summary

In this chapter, the scaling issues of tunnel FET have been discussed, and it is shown that they follow different scaling rules in comparison to the conventional MOSFETs. Further,

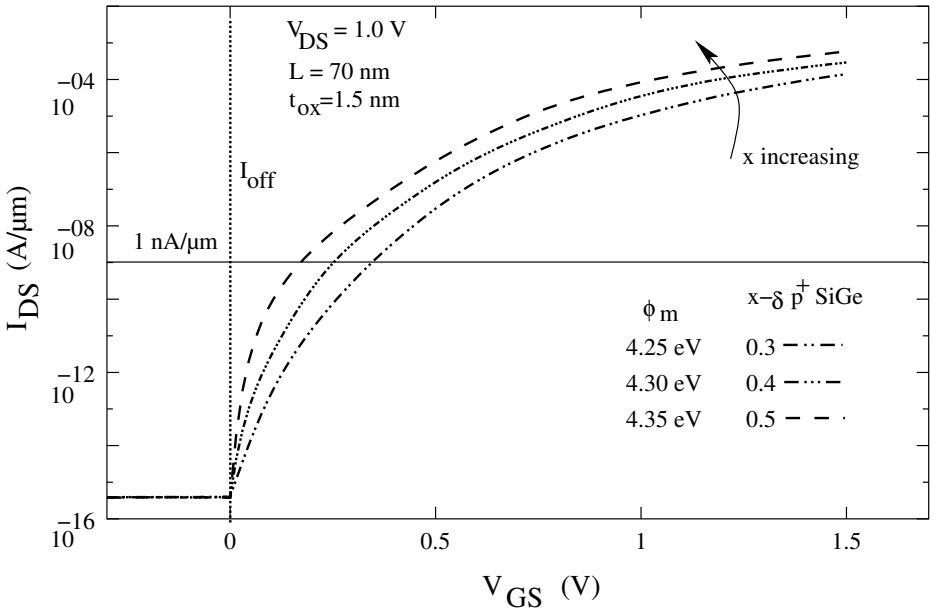

Figure 4.20: *N-channel transfer characteristics for tunnel FET with $x = 0.3$, 0.4, and 0.5 ($L = 70$ nm, $t_{ox} = 1.5$ nm) with appropriate gate workfunction engineering.*

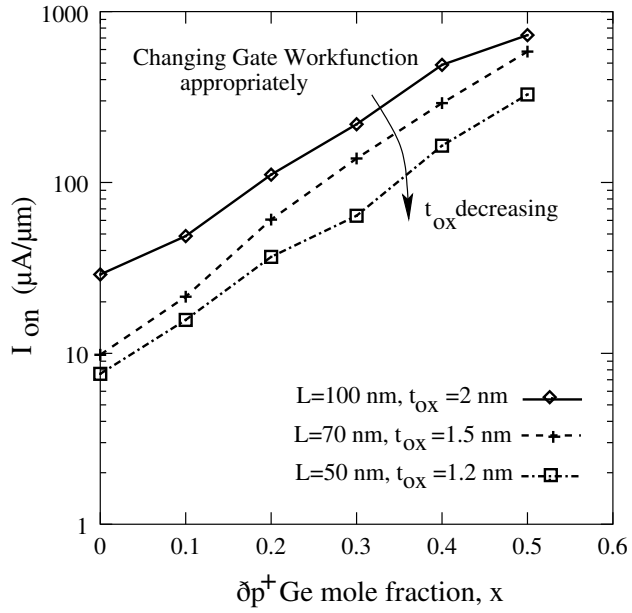

Figure 4.21: *I_{on} for tunnel FETs as a function of Ge content, x, L and t_{ox} scaling and appropriate gate workfunction engineering. Increase in I_{on} for all values of x and ϕ_m reveals that the loss in I_{on} is not significant.*

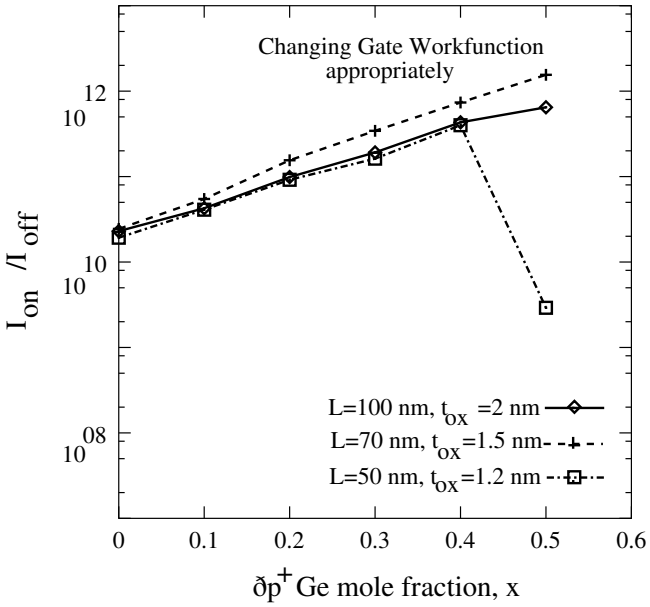

Figure 4.22: *I_{on}/I_{off} ratio for tunnel FETs as a function of Ge content, x, L and t_{ox} scaling and appropriate gate workfunction engineering.*

while the device performance does not improve with both t_{ox} and L scaling, SiGe provides an additional parameter for the purpose. Large tunneling leakage current at zero gate bias with SiGe can further be lowered by gate workfunction engineering. Thus, the proposed tunnel FETs look very good for both high-speed applications as well as low operating power for future CMOS technologies. In the following chapter, experimental results for the silicon tunnel FETs are demonstrated.

Chapter 5

Experimental Results

In this chapter, experimental verification of the silicon tunnel FET characteristics down to the 25 nm channel length is presented. Vertical tunnel FETs with 'i'-Si layer of 70 nm and 25 nm, and t_{ox} of 4.5 nm are processed under identical conditions in order to study the scaling properties of these devices. While the leakage current I_{off} increases significantly for the 25 nm device due to the p-i-n diode Zener breakdown, the on-current is found to be independent of L. The tunnel FET current-voltage characteristics is shown to have a weak temperature dependence. Further, the modified Kane's model, as discussed in chapter 2 is shown to give a good match for this device. A temperature independent swing down to 34 K, and strong $V_{GS} - S$ dependence is further confirmed.

5.1 Device Fabrication Method

In this section, a brief discuss the fabrication method of the tunnel FET is done. The vertical layer stack is grown on a commercially available AMAT Centura tool by LPCVD on a $3{\times}10^{18}$cm^{-3} p-substrate ($\rho = 20$ mΩ-cm). A 25 nm 6-8$\times10^{19}$cm^{-3} boron doped (active) layer is grown to form the p-source region, followed by the i-Si layer which determines the channel length of the device. The i-Si layer is 70 nm and 25 nm for the two devices. $8{\times}10^{19}$cm^{-3} doped arsenic (active) silicon layer is grown on top which also forms the drain electrode. Thus forming a gated p-i-n diode. After mesa etching, 4.5 nm silicon oxide is thermally grown by wet oxidation at 800^{o}C for 5 minutes. 300 nm p$^+$ polysilicon is deposited by LPCVD to form the gate electrode. Fig. 5.1 shows the schematic representation of the device. The tunneling junction for the n-channel and p-channel operating mode, and the channel length are indicated. Fig. 5.2 shows the tunneling electron microscope (TEM) image of the vertical structure grown in our institute. The various regions corresponding to the tunnel FET are indicated. The arsenic and boron secondary ion mass spectroscopy (SIMS) doping profile of the two devices with the i-Si layer[1] of 70 nm and 25 nm are shown in figures 5.3 and 5.4, respectively. Detailed experimental fabrication method of these devices is not the scope of this work and will be discussed elsewhere [131].

[1]It should be noted, that the smear-out of the dopants lead to a high doping in the channel. Since the tunnel FET parameters are independent of L, the intersection point of the two doping profiles (boron and arsenic) in the channel, than becomes a critical parameter. The doping density at the intersection (seen to increase for lower i-Si layer) result in degraded performance. Ideally, it is not L which determines the device performance, but the intersection point of the doping profiles, and need for a sharp doping profile for tunnel FETs thus, becomes very critical.

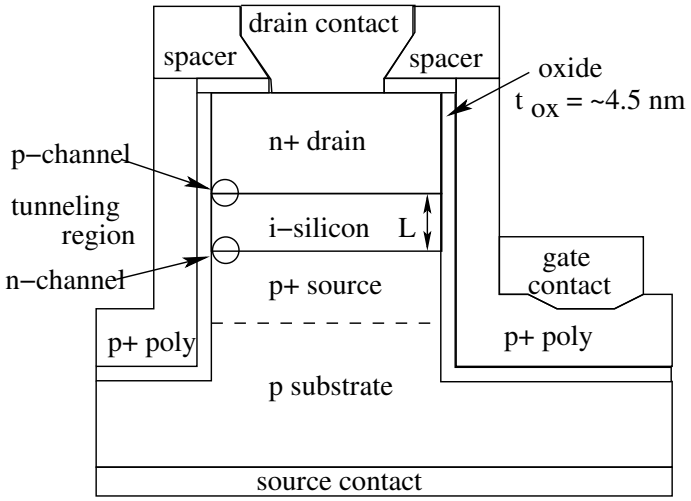

Figure 5.1: *Schematic representation of the tunnel FETs. The tunneling region for both n-channel as well as p-channel operating mode are shown.*

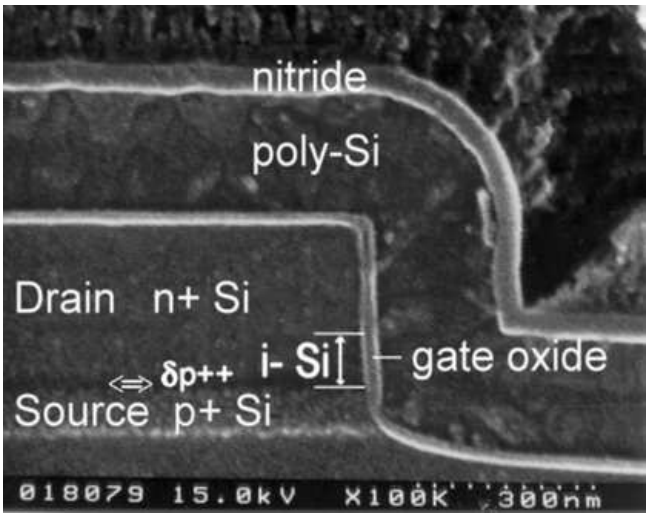

Figure 5.2: *A tunneling electron microscope (TEM) image of a vertical MOSFET structure fabricated in our group. The various doping regions of the tunnel FET are marked.*

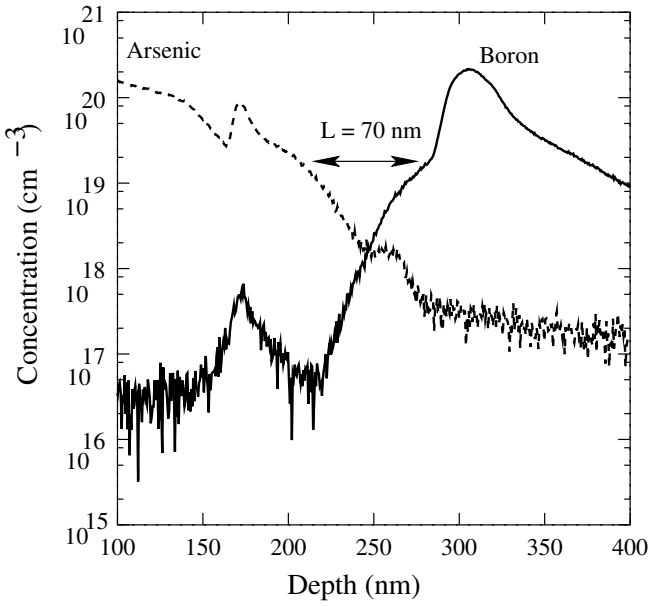

Figure 5.3: *SIMS doping profile of the 70 nm tunnel FET grown by LPCVD.*

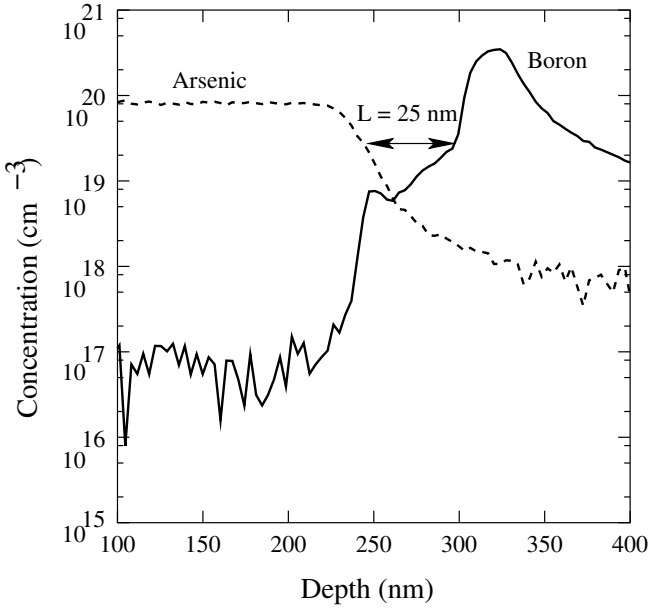

Figure 5.4: *SIMS doping profile of the 25 nm tunnel FET grown by LPCVD.*

5.2 Electrical Characteristics

Since the devices were fabricated with p^+ polysilicon gate material, they are optimized for p-channel performance. Symmetric and highly doped source and drain doping profiles result in both p-channel as well as n-channel tunnel FET behavior. The devices were characterized using a HP4155 semiconductor parameter analyzer and all measurements were taken under dark conditions. For p-channel transfer characteristics ($V_{GD} < 0$ V), the gate-drain bias is varied from 0.0 to -5.0 V in steps of 50 mV, while for the n-channel transfer characteristics ($V_{GS} > 0$ V), the gate-source bias is varied from 0.0 V to 5.0 V in step of 50 mV. The p^+source is always kept at ground potential, while the n^+drain is biased from 0.0 to 1.0 V in steps of 0.3 V. For the output characteristics, both forward-biased as well as reverse-biased behavior is investigated. The drain bias is varied from -1 V to 1.5 V for 70 nm tunnel FET. Since the oxide thickness is 4.5 nm, the gate bias is limited to 4.5 V. Low temperature measurements are taken by a helium closed-cycle down to 33 K, while high temperature measurements are taken upto 100 ^{o}C.

5.2.1 Transfer Characteristics

Fig. 5.5 shows the room temperature p-channel transfer characteristics of the 70 nm tunnel FET with $W = 2$ μm (sample no. J10N1[2]). The various electrical parameters shown in the figure are: V_T at $I_{DS} = I_{VT} = 0.1$ μA/μm; $V_{off} = V_{GD}$ at which the reverse-biased p-i-n diode characteristics undergo a transition to that of a tunnel FET, and V_{on} is the gate-potential corresponding to $|V_{GS}|/t_{ox} = 1$ V/nm.

Exponentially increasing transfer characteristics is observed for both the on-region as well as the off-region of operation. There is an initial strong drain dependence and than the curves reach quasi-saturation. I_{DS}, at $V_{GD} = 0.0$ V and $V_{DS} = 0.7$ V is 560 fA resulting in an off-current of 280 fAμm. At $V_{GD} = 4.5$ V and $V_{DS} = 0.7$ V, I_{DS} is 2.09 fA resulting in an on-current of 1.045 μA/μm. Thus, the device shows an excellent I_{on}/I_{off} ratio of 3.7×10^6. The on-current is several orders of magnitude higher than previously reported for vertical tunnel FETs. It should further be noted, that while I_{on} is 3 orders of magnitude lower than the ITRS requirements, it is the highest achieved for vertical tunnel FETs. I_{off}, on the other hand, is several orders of magnitude less than the technology requirements for the 70 nm node.

Beyond $V_{DS} = 0.7$ V, the p-i-n diode Zener breakdown leads to significant increase in tunneling leakage currents. Since the device has a t_{ox} of 4.5 nm, the device has a high V_T of -3.4 V at $I_{DS} = I_{VT}$. The V_T can further be lowered by lowering the t_{ox}. As the gate controlled tunneling probability is insignificant at $V_{GD} = 0$ V, I_{off} for this device is determined by the bulk p-i-n diode leakage current and is thus, independent of t_{ox} scaling. Furthermore, as can be seen from the figure V_{off} is nearly -0.9 V at $V_{DS} = 0.7$ V. Thus, the V_T can further be lowered by gate workfunction engineering. This will result in improved I_{on} without loss in I_{off}. The gate leakage current is also shown in the figure and is seen to be small compared to I_{DS} for all values of V_{DS}.

Fig. 5.6 shows the room temperature n-channel transfer characteristics for the device. Due to p^+polysilicon gate electrode, the n-channel device has a high V_T and V_{off} values. While I_{off} remains at the bulk p-i-n diode leakage current of 280 fA/μm, I_{on} is 35 nA/μm. Choice of a mid bandgap gate material will result in asymmetric current-voltage characteristics.

[2]The sample number corresponds to the number on the wafer: J10 is the chip number, N1 is the transistor.

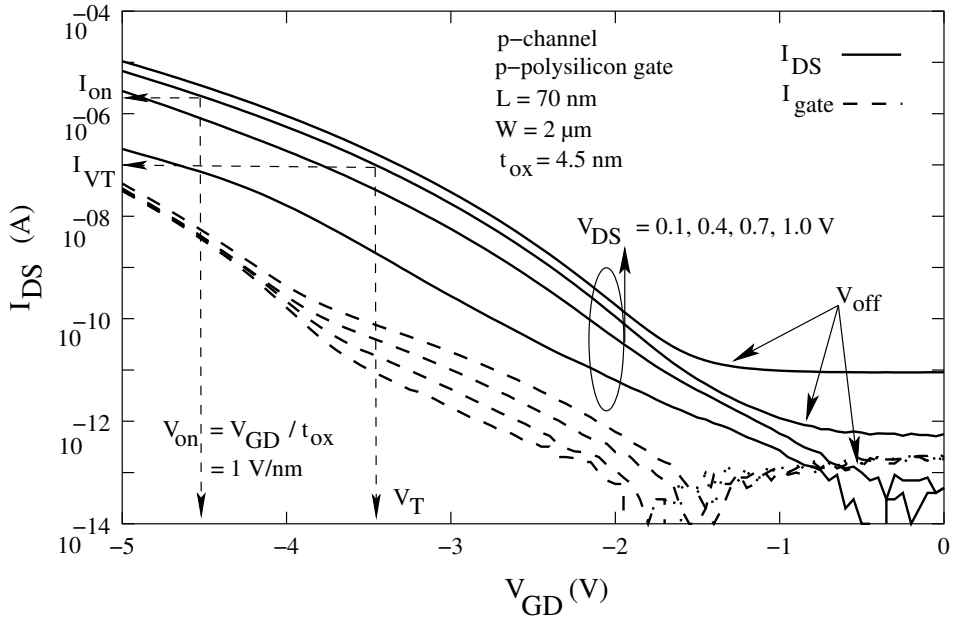

Figure 5.5: *P-channel transfer characteristics of a 70 nm channel length tunnel FET (J10N1). The gate leakage current is also shown. The various electrical parameters are marked on the figure.*

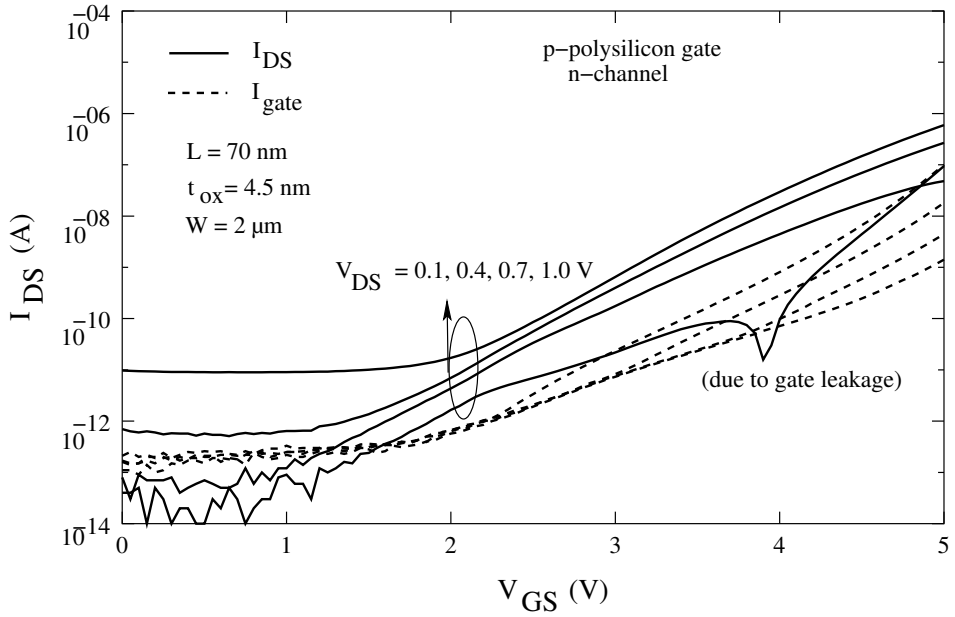

Figure 5.6: *N-channel transfer characteristics of the 70 nm channel length tunnel FET (J10N1).*

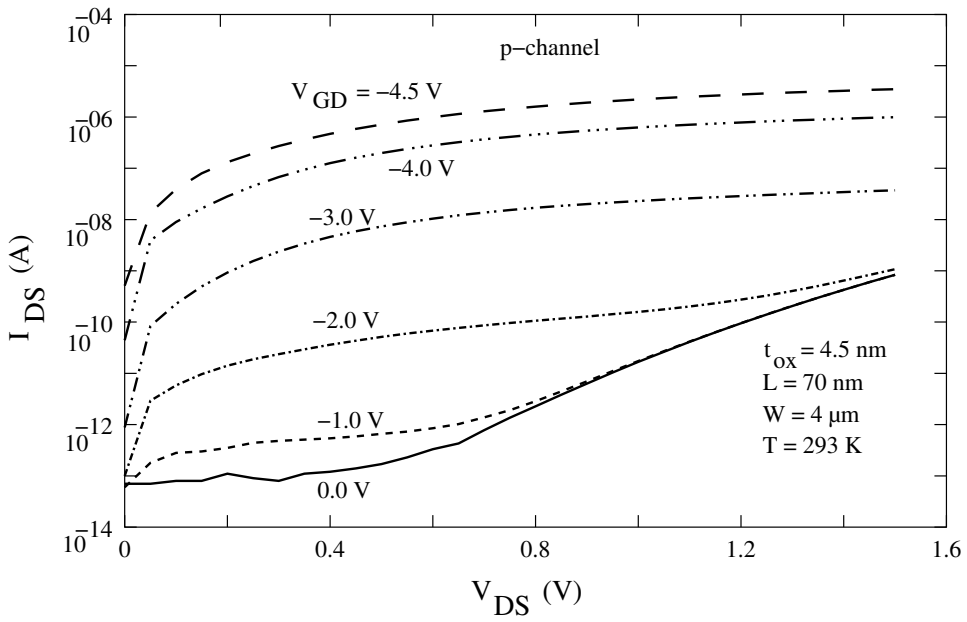

Figure 5.7: *P-channel output characteristics of a tunnel FET (G7B2) with L =70 nm and t_{ox} = 4.5 nm. Due to a thick oxide, no saturation behavior is observed.*

5.2.2 Output Characteristics

The room temperature reverse-biased output characteristics are shown in Figures 5.7 and 5.8 for the p-channel and the n-channel operating modes respectively (sample no. G7B2). The devices do not show a good saturation behavior due to a thicker oxide, and the characteristics only reach a quasi-saturation behavior like the earlier demonstrated tunnel FETs [83, 84]. At zero gate bias, the p-i-n diode Zener breakdown is observed at 0.7 V beyond which the diode current starts to increase exponentially. Since I_{off} is limited by the bulk p-i-n diode current, this can further be lowered by decreasing the vertical mesa width.

5.2.3 Forward-biased p-i-n diode

The room temperature forward diode characteristics of the device are shown in figures 5.9 and 5.10 for p-channel and n-channel respectively. At zero gate bias, normal p-i-n diode characteristics are observed. Even though the devices have a high source and drain doping, no NDR is observed. As V_{GS} is increased, strong exponential gate and drain dependence is observed even in the forward-bias (Fig. 5.11). Further, the curves does not show Esaki tunneling related NDR characteristics as has been reported earlier for surface tunnel FETs in both III-V compounds [76] and silicon [77, 78]. Since surface Zener tunneling probability is small when the diode is forward-biased, and vanishes above the degenerate doping levels, which is less than 0.2 V in silicon, the tunneling current observed here is not expected to be of Esaki origin.

However, when the p-i-n diode is 'off' (for[3], $V_{DS} < 1.1$ V which is the bandgap of silicon), there could be a significant gate induced tunneling probability in the dopant smear-out region

[3]This depends on the doping in the source and drain regions. For degenerate doping, it is nearly equal to the bandgap of silicon.

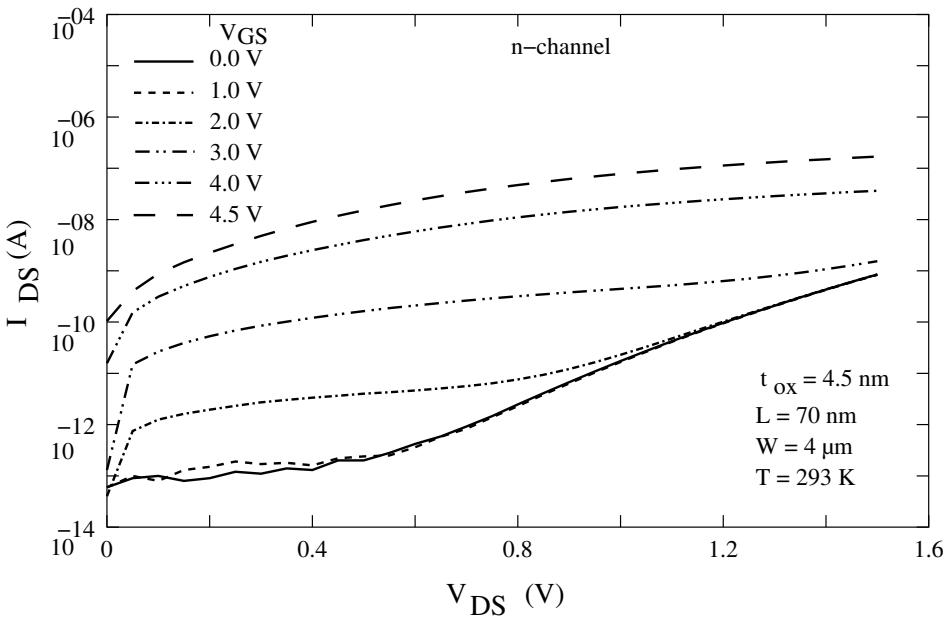

Figure 5.8: *N-channel output characteristics of the tunnel FET with $L = 70$ nm and $t_{ox} = 4.5$ nm. Similar characteristics is observed as for the p-channel tunnel FET.*

in the channel. This is possible, as it can be seen from the SIMS doping profile of the device, though the source and drain dopings are quiet high they are not very sharp and abrupt at the junctions. Thus, the gate bias will result in band-bending in the channel in the smear-out regions, resulting in significant gate-induced tunneling 'leakage' currents. Further, when the p-i-n diode is 'on' (for $V_{DS} > 1.1$ V) the tunneling probability falls to zero, and only resistive forward current is observed.

The situation is best described by looking at the *differential* forward current, I_{Diff} defined as,

$$I_{Diff} = I_{DS} - I_{DS-o} \tag{5.1}$$

where I_{DS} is the forward drain current for an applied gate bias, and I_{DS-o} is the forward drain current at $V_{GS} = 0.0$ V, that is, when the tunneling probability is low. Ideally, I_{DS-o} can be defined as the diode current under flat-band conditions, or the *bulk* diode current. Thus, Figures 5.12 and 5.13 show the I_{Diff} as a function of V_{DS} for p-channel as well as the n-channel operating mode respectively. The curves are plotted in the linear scale. Clear peaks are observed at V_{DS} corresponding to the diode 'on' voltage. Since the peak V_{DS} is *same* for both p-channel as well as the n-channel device, it further justifies the explanation. The increase in peak current with increase in V_{GS} is due to the higher tunneling current with increase in V_{GS}.

Thus, the forward current becomes a quality assessment parameter for the tunnel FETs. Peak differential current[4] has been reported at voltages of 0.5 to 0.7 V [87, 132] and 0.85

[4]It should be noted that in all the earlier work, for both lateral as well as vertical structures, it has been explained in terms of Esaki or resonant interband tunneling. However, the peak is always observed at significantly higher V_{DS}. Furthermore, I_{DS} is *exponentially* increasing for *both* V_{GS} and V_{DS}. Thus, Esaki tunneling is not likely to be the reason for the peaks observed in these devices.

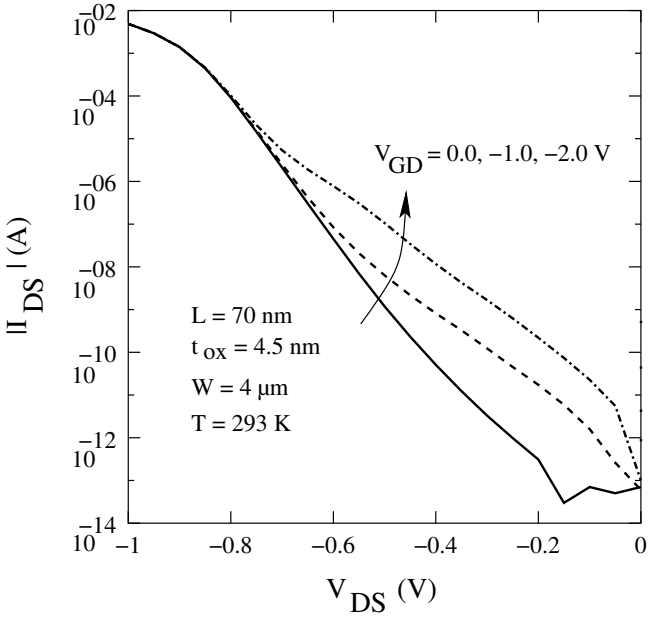

Figure 5.9: *P-channel forward-characteristics of the gated p-i-n diode at room temperature. The device shows a strong gate dependence.*

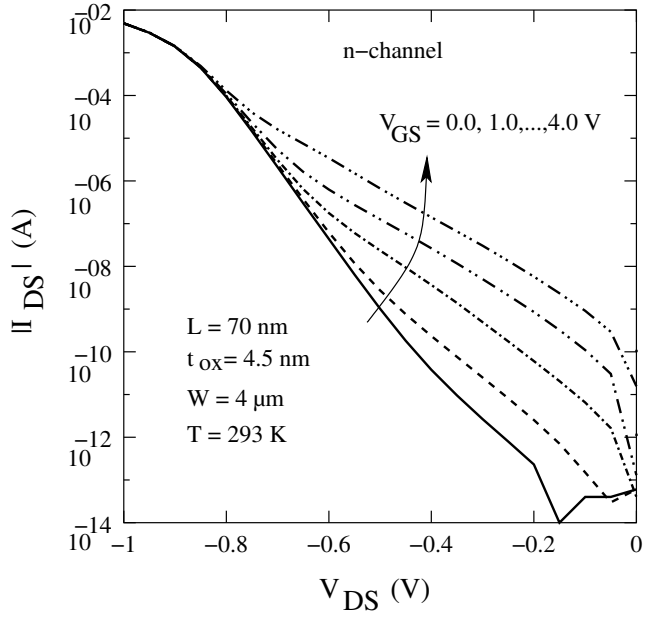

Figure 5.10: *N-channel forward-characteristics of the gated p-i-n diode at room temperature. Gate dependence, similar to the p-channel device is observed.*

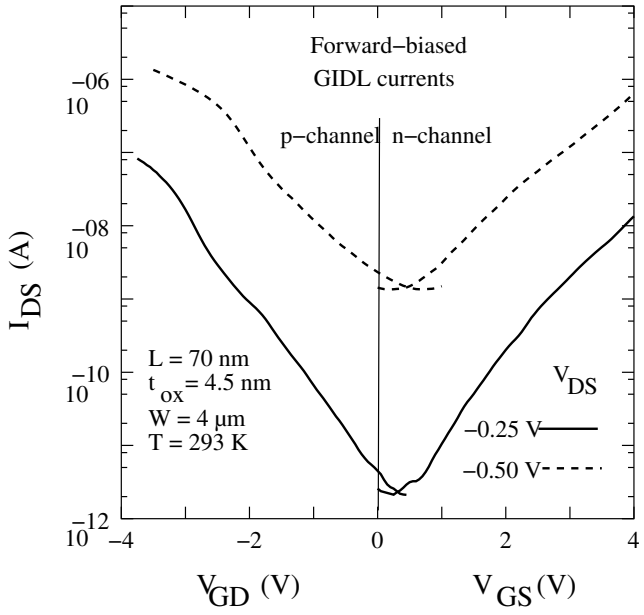

Figure 5.11: *Forward drain current as a function of V_{GS} for V_{DS} = -0.25 V and -0.50 V. The current is exponentially increasing with both increase in V_{GS} and V_{DS}.*

V [86, 133]. This is attributed to the low doping profile in the source-drain regions. For an ideal tunnel FET, with an extremely high and abrupt doping in the source and drain, the forward current will not show tunneling currents from the overlap regions. The device characteristics is then similar to the simulated $I_{DS} - V_{DS}$ curve shown in Fig. 2.14.

However, for very thin mesa structures which in turn suppress the bulk p-i-n diode current, Esaki tunneling current might be possible. This is the scope of future work.

2-D simulations reveal similar behavior. Fig. 5.14 shows the simulated forward-biased current for the gated p-i-n diode ($L = 100$ nm, $t_{ox} = 2$ nm). The uniform and abrupt source doping is chosen to be $1\times10^{19}\text{cm}^{-3}$ while the drain is at $1\times10^{20}\text{cm}^{-3}$. At zero gate bias, forward gate current is observed. As V_{GS} is increased, tunneling from the gate overlap reion of the source lead to an increase in the diode current. The differential current reveals similar peak as observed with experimental results (Fig. 5.15). However, due to the uniform doping profile, in strong inversion, the bands saturate leading to a saturation in the diode current with gate bias. Since, for the experimenatl devices, the source doping is high and tunneling is believed to be taking place in the smear-out regions in the channel, the characteristics does not show shaturation behavior. In a recently demonstrated lateral n-channel tunnel FETs [87, 88], saturation in the *transfer* characteristics has been reported. Further, in the forward-biased NDR is observed with a peak voltage, V_p of 0.6 V. As it has been mentioned by the authors, the drain doping is kept low, in order to have the p-channel device 'off' when the n-channel is 'on', the V_p of 0.6 V, could well correspond to the diode on-voltage.

5.2.4 Temperature Dependence

In this section, temperature dependence on the tunnel FET parameters, both at low temperatures as well as high temperatures is investigated. In chapter 2 it was claimed that the tunnel FET performance is weakly dependent on temperature and swing is independent of

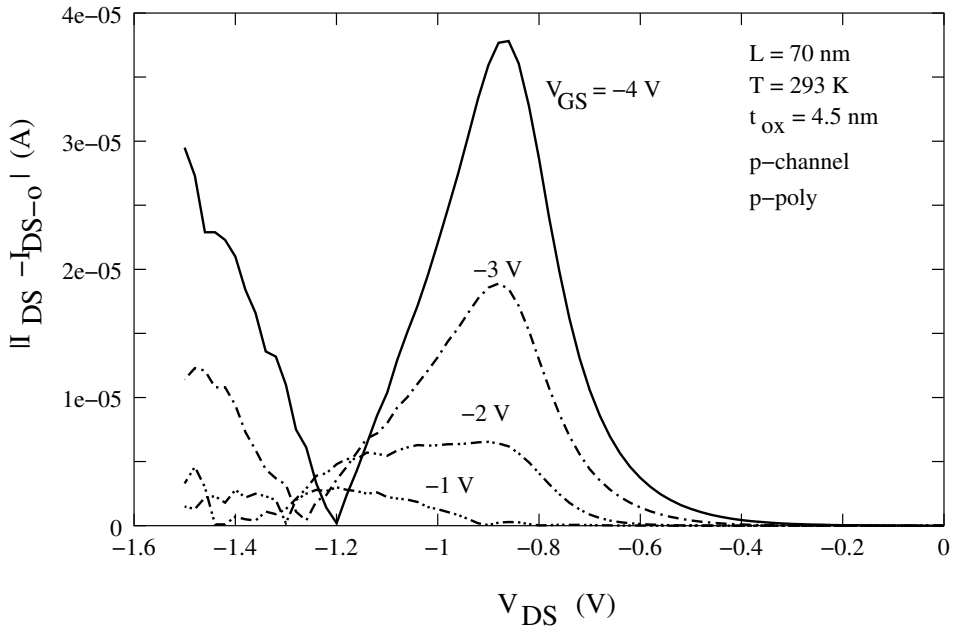

Figure 5.12: *Forward-biased differential current as a function of V_{GS} for the p-channel device.*

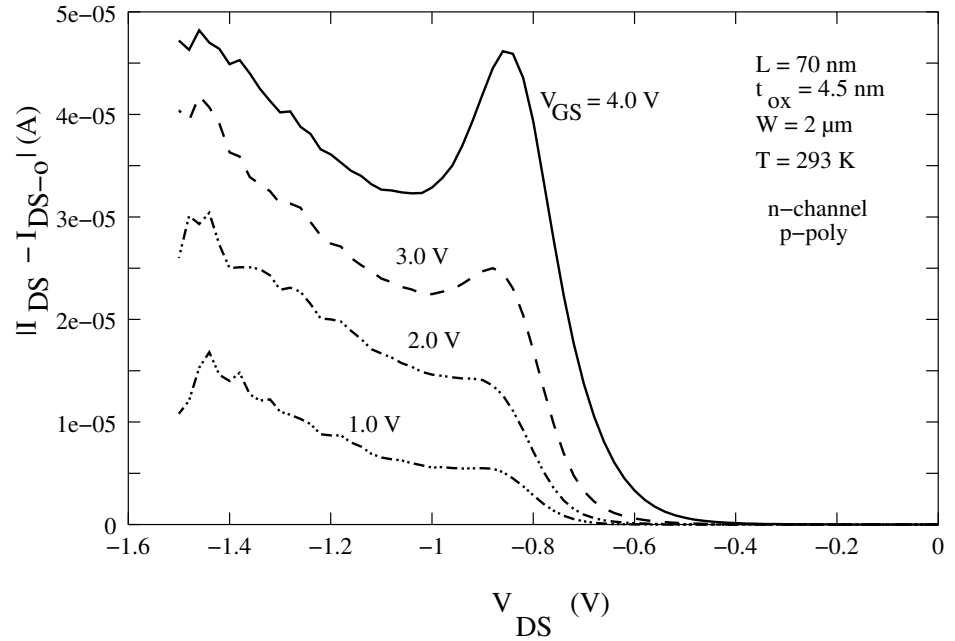

Figure 5.13: *Forward-biased differential current as a function of V_{GS} for the n-channel device.*

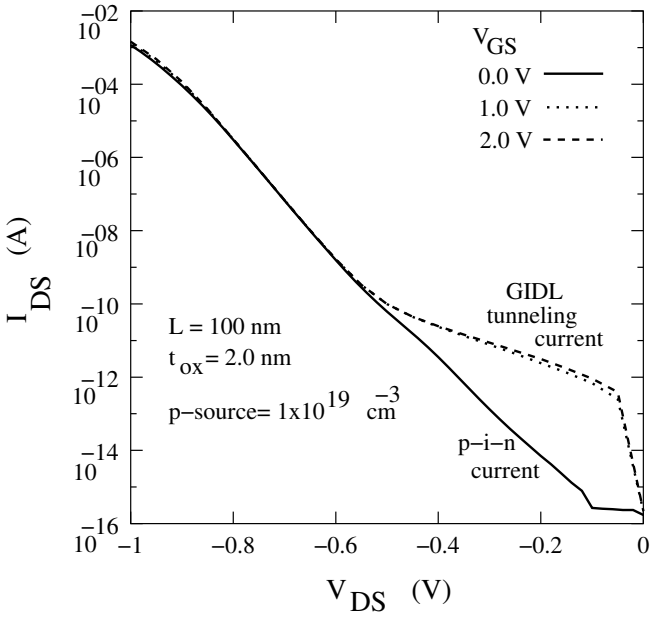

Figure 5.14: *Simulated forward-biased current as a function of V_{GS} for the n-channel device. The source doping is chosen to be constant at $1\times10^{19}cm^{-3}$.*

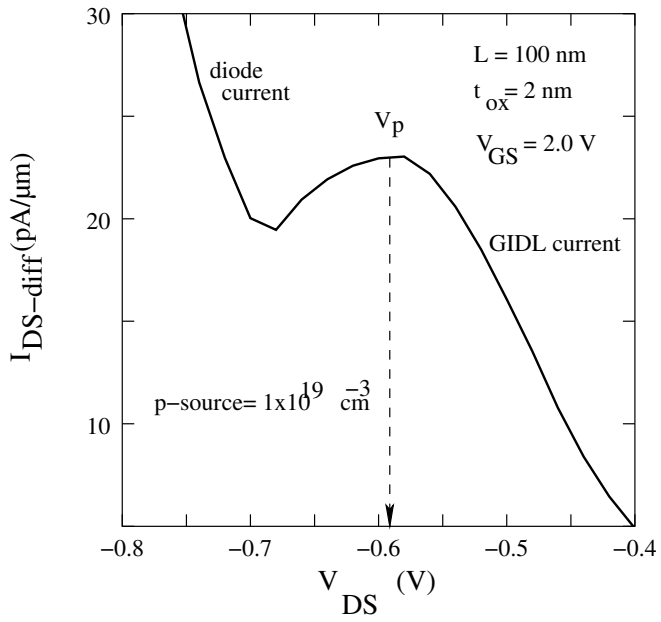

Figure 5.15: *Simulated differential forward-biased current for the diode current of Fig. 5.14 at $V_{GS} = 2.0$ V.*

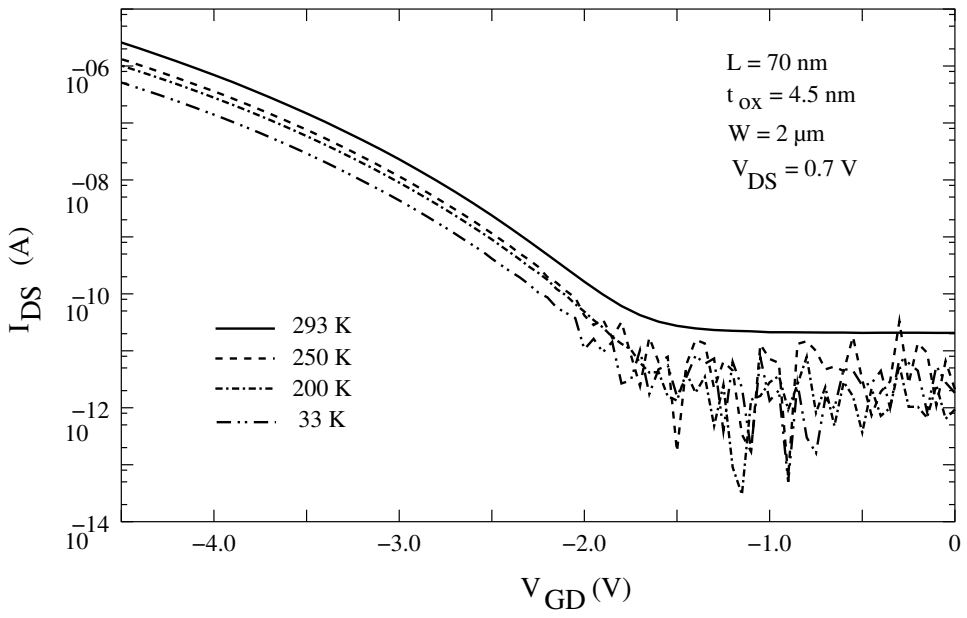

Figure 5.16: *Low temperature transfer characteristics of a 70 nm tunnel FET.*

the kT/q thermal factor. This is confirmed here by means of experimental results. Fig. 5.16 shows the transfer characteristics of the p-channel tunnel FET (I9A1) as a function of temperature at $V_{DS} = 0.7$ V ($W = 2$ μm, $L = 70$ nm). T is varied from room temperature 293 K to 33 K. As can be seen, with lowering T, as expected, the bulk p-i-n diode current, I_{bulk} is seen to lower, while the tunneling current, I_{b2b} is nearly independent of temperature. Thus, I_{on} is lowered by only a factor of 5 for T lowering from 293 K to 33 K. Further, the swing, S is also seen to be independent of T and hence the kT/q factor.

The high temperature transfer characteristics are shown in Fig. 5.17 for T increasing from 25°C to 100°C (G7H3). While I_{on} is seen to increase only by a factor of 2.

Thus, as expected, the tunnel FET current-voltage characteristics are essentially independent of temperature, T. This is advantageous, as the device can be reliably operated at both low as well as high temperatures.

5.2.5 Swing-V_{GS}

In this sub-section, experimental verification of the strong $V_{GS} - S$ dependence is given. As it has been shown by means of 2-D computer devices simulations in chapter 3, the swing of a tunnel FET is a strong function of V_{GS}. This is due to the fact that the current-voltage characteristics follow an exponential behavior with V_{GS} in the exponent.

In chapter 2 it was showen that the modified Kane's model give a good match with the experimental characteristics for our earlier demonstrated tunnel FET with $t_{ox} = 16$ nm and $L = 100$ nm. The same is confirmed for the tunnel FET with $t_{ox} = 4.5$ nm and $L = 70$ nm, for the device demonstrated in this chapter. This is shown in Fig. 5.18 where the normalized drain current as a function of inverse-V_{GS} is plotted in the tunneling region (G7A2). Good match with the modified Kane's model is achieved for the device. Thus, justifying the approach used for our simulations. Using the modified Kane's model, it was proposed that the swing is not a constant in the subthreshold region, but a strong function of V_{GS}. For

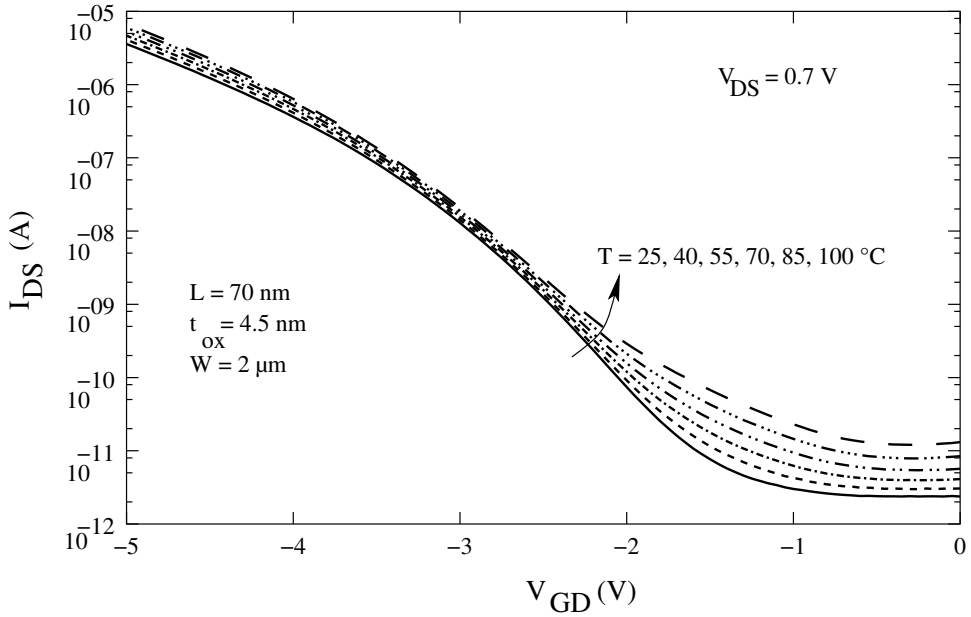

Figure 5.17: *High temperature transfer characteristics of a 70 nm tunnel FET.*

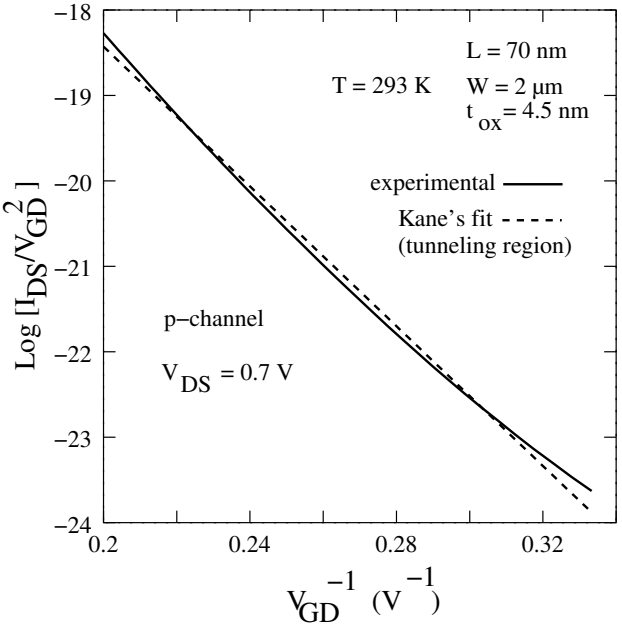

Figure 5.18: *Exprimental verification of the modified Kane's model. The reverse-biased tunneling current is plotted only as a function of V_{GS} in the quasi-saturation region.*

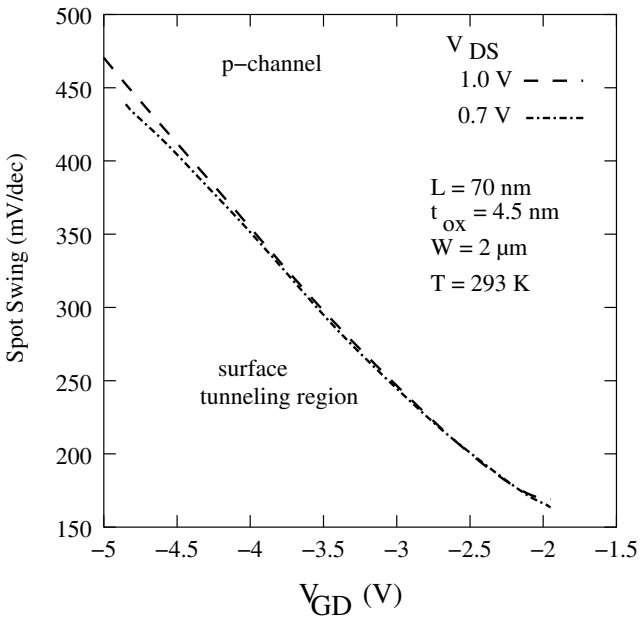

Figure 5.19: *Experimental 'spot' swing, S as a function of V_{GS} for V_{DS} = 0.7 V and 1.0 V. S is seen to be independent of V_{DS} in the quasi-saturation region.*

very small V_{GS}, 'spot' S can be very small tending to zero. Fig. 5.19 shows the experimental 'spot' value of swing as a function of gate bias, V_{GD} in the quasi-saturation region for V_{DS} = 0.7 V and 1.0 V. As predicted, S is seen to increase significantly with increasing V_{GS} for both the off-region as well as the on-region of operation. Furthermore, 'spot' swing is seen to be *independent* of V_{DS}. At large V_{GS} it is seen to degrade with V_{DS} due to lowering in the channel resistance which results in degrading gate control over the device. The minimum 'spot' value of S observed here is nearly 160 mV/dec at V_{GD} = -2.0 V. This is because the V_T of this device is high resulting in a high V_{off}. This also results in a high effective subthreshold swing for this device. The parameters can further be optimized by having a thinner oxide thickness and sharper doping profiles in the source and drain regions.

5.2.6 25 nm Channel Length Tunnel FET

Finally, in this sub-section, the electrical characteristics of a p-channel 25 nm tunnel FET is discussed. The device transfer characteristics are shown in Fig. 5.20. As the device is processed under identical conditions as compared to the 70 nm tunnel FET, I_{on} is observed to be identical to the 70 nm device. This is consistent with the simulation results and also the tunneling theory that tunneling currents are independent of L scaling up to 10 nm in Si. Furthermore, this is the first experimental demonstration of an experimental sub-50 nm tunnel FET. However, due to smeared-out doping profile and small channel length, the device shows an early Zener breakdown, resulting in an exponentially increasing I_{off} with increasing V_{DS}.

The device can further be optimized by having a sharper doping profile which will result in improved Zener breakdown potential resulting in improved I_{off}.

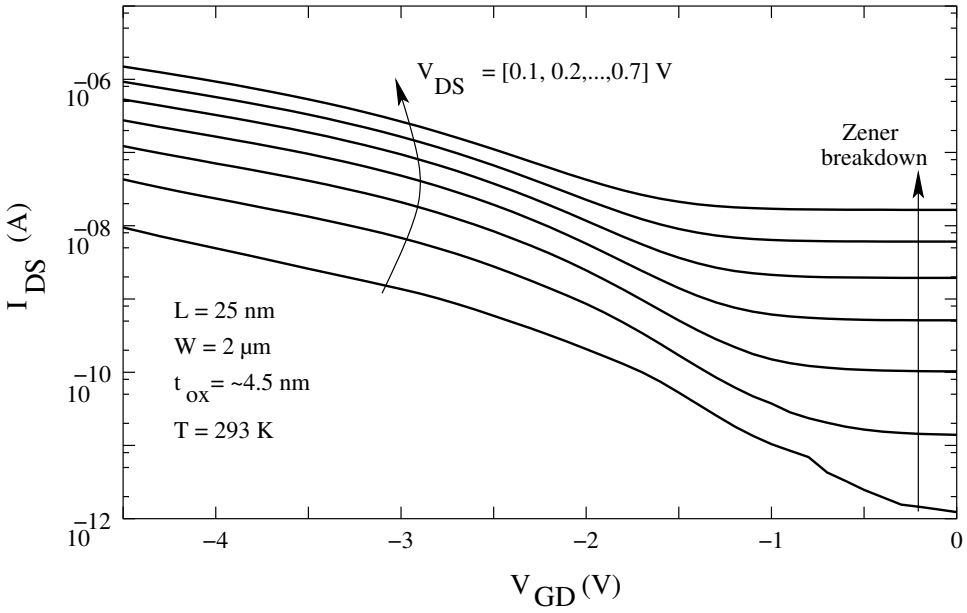

Figure 5.20: *Transfer-characteristics of a 25 nm p-channel tunnel FET.*

5.3 Summary

In this chapter, experimental results of a tunnel FET fabricated in our group are presented and the various electrical parameters of the device down to the 25 nm channel length are verified. Though the devices are fabricated with p-polysilicon gate material, both p-channel as well as n-channel behavior is observed. Due to a symmetric doping profile, the device characteristics show similar behavior. Though these devices show a high I_{on}/I_{off} ratio and a highest on-current ever reported for vertical tunnel FETs, they do not show good saturation behavior. Furthermore, the I_{on} is only a factor of 10 less than that predicted by simulation for the silicon tunnel FET. This is due to a relatively high t_{ox} of 4.5 nm. As it was shown in earlier chapters, the saturation behavior will improve with lowering the t_{ox}.

Forward-biased current shows gate dependence resulting from tunneling from the smeared-out doping profile. Thus, the tunnel FET performance can further be improved by having a sharper doping profile. This is the scope for future work.

Chapter 6

Symmetric High-Performance Tunnel FET

The vertical MOSFET structures provide an interesting research tool for understanding the MOSFETs behavior down to very short-channel structures as well as to experiment innovative ideas and devices. However, limitations like the large overlap gate capacitances, and no promising solution for circuts design, they have not been integrated into the mainstream industrial research. Further, as has been discussed earlier in this this thesis, the silicon tunnel EFT failed to meet the technology requirements in terms of on-current. Improvements with δ-doped SiGe resulted in significant improvement in the n-channel device, however the p-channel performance remained unaffected. This is due to the fact that with pseudomorphic strained SiGe, only the valence band is raised relative to the conduction band. Thus, in this chapter a proposal of a new high-performance lateral tunnel FET with potential for symmetric n- and p-channel behavior is made.

6.1 Lateral Tunnel FETs

Lateral tunnel FETs on silicon [72] as well as on silicon-on-insulator (SOI) [1] [74] have been proposed. Recently, silicon lateral tunnel FETs down to the 90 nm channel length have been demonstrated [135][2] The devices though showed good saturation behavior and low off-current, had low on-current in comparison to the technology requirements. Though the earlier proposed vertical tunnel FET with δ-SiGe layer, showed improvement in the n-channel performance, the p-channel performance remained unaffected. However, both, a high on-current as well as very low off current were achieved. In the following, it is shown that the performance of the lateral tunnel FET on SOI can be improved by having a pseudomorphically strained SiGe layer. However, the off-current also increases with increasing Ge content, x, as the intrinsic carrier concentration increases.

[1] For a quick review of SOI devices, see J. P. Collinge [134]

[2] A careful analysis of the results reveal that the device characteristics do not resemble that of gated p-i-n diode tunnel FET, as claimed by the authors. Since it is processed under *standard* CMOS process flow, due to the dopings in the source, drain and channel regions the device is a combination of a *conventional MOSFET* and a gated p-n junction. This is revealed in the output characteristics of the device, and low temperature measurements which show a strong channel dominant characteristics. To this authors best understanding, the device essentially is a conventional MOSFET.

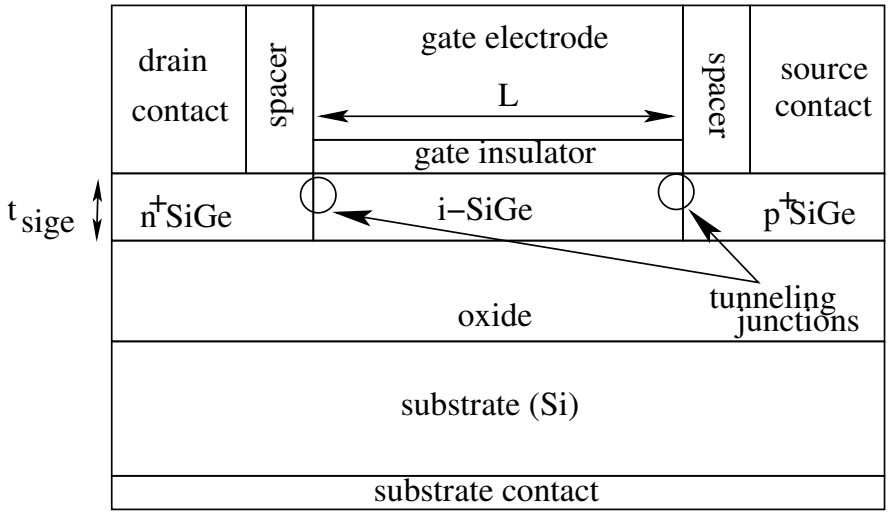

Figure 6.1: *Schematic representation of a lateral high performance symmetric tunnel FET. The workfunction can be adjusted in a way to have either n-channel or p-channe tunnel junction small.*

6.1.1 Device Structure

Fig. 6.1 shows the device structure of the lateral tunnel FET with SiGe-on-insulator (SiGeOI). The device can be fabricated by a self-alligned process used in conventional MOSFETs. The source and drain are heavily doped p and n-type respectively. The regions can be formed either by selective epitaxy or by ion-implantation. The gate insulator material can be deposited by LPCVD, either oxide or relevent high-κ gate material. The gate electrode can be chosen to adjust the workfunction of the device in order to optimize the performance, as discussed in chapter 4.

6.1.2 Current-Voltage Characteristics

Fig. 6.2 shows the simulated n-channel transfer characteristics for the proposed lateral tunnel FET, as a function of Ge content, x increasing. The channel length, L, and oxide thickness, t_{ox}, are chosen to be 100 nm and 2 nm, respectively. The SiGe layer thickness is chosen to be 10 nm here. The p^+source and n^+drain doping is kept at $1\times10^{20}cm^{-3}$, while the i-region is intrinsic. A thicker layer will only result in increases bulk p-i-n diode current, while leaving the surface tunneling current unaffected. The performance improvement is similar to that observed with δp^+ SiGe layer for the n-channel vertical tunnel FETs. However, I_{off} increase with increasing in x due to the increase in the intrinsic carrier concentration, as the bandgap of SiGe layer is reduced with increasing x (Eq. 3.1). This results in increased diffusion leakage current, I_{bulk} and hence I_{off}.

Fig. 6.3 shows the simulated p-channel transfer characteristics for the device. While the n-channel tunnel FET has n-polysilicon gate, p-polysilicon gate is used for this device. Similar performance improvement is observed for this device in terms of both n-channel as well as p-channel performance. However, the device shows a higher V_T. The performance for both the n-channel as well as p-channel can be matched with proper workfunction to have

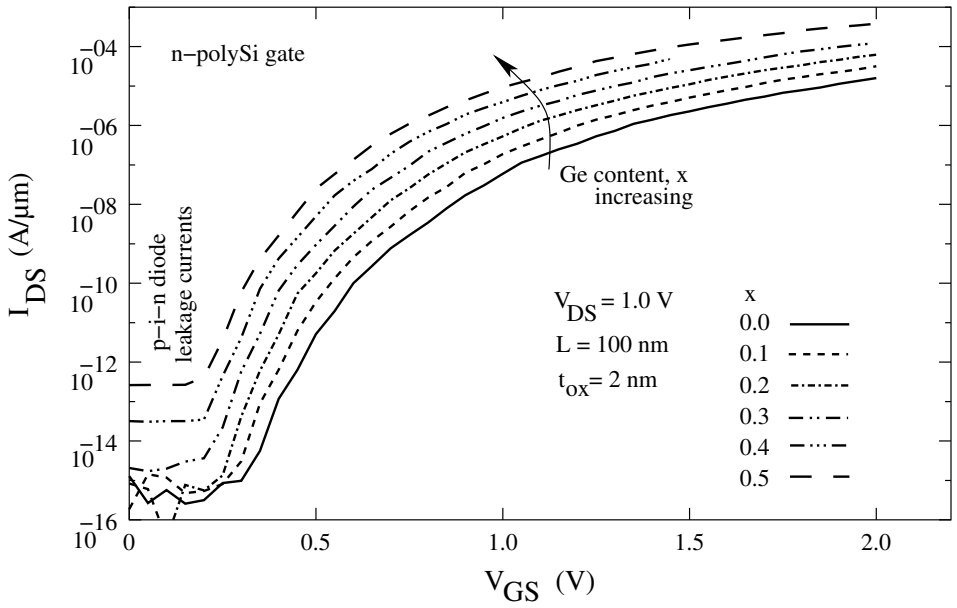

Figure 6.2: *Transfer characteristics for an n-channel lateral SiGe-on-insulator tunnel FET wiht increase in Ge content, x (L = 100 nm, t_{ox} = 2 nm, n-polysilicon gate).*

the same characteristics.

Fig. 6.4 shows the transfer characteristics for t_{sige} changing from 20 nm to 2 nm. As the current is a surface tunneling current, there is not much change in the characteristics. Thus, the performance is essentially invarient of the SiGe thickness. For very small t_{sige}, however, quantum mechanical effects may limit the performance. This has to be investigated in future work.

6.2 Summary

In this chapter, a very brief discussion of a lateral high performance tunnel FET on SiGe-on-insulator is done. The device performance is shown to improve with the Ge content, x, increasing for both the n-channel as well as p-channel performance. However, the leakage current, I_{off}, increases with increasing x as the intrinsic carrier concentration, n_i, increases with lowering of W_g with x increasing. However, it still remains below the technology requirements. Future work includes a detailed study of the parameters of this device and optimization to achieve symmetric performance with respect to n-channel as well as p-channel.

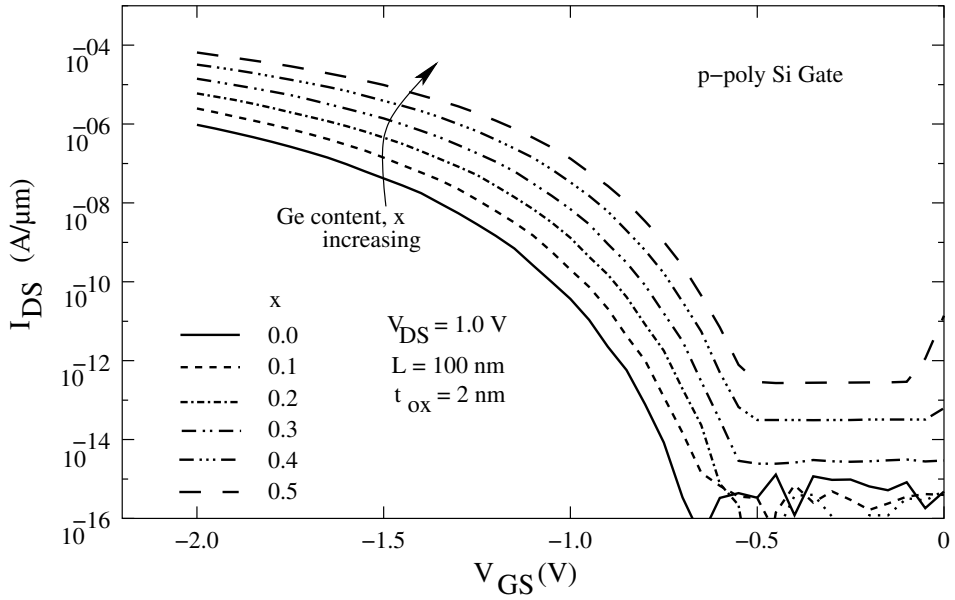

Figure 6.3: *Transfer characteristics for a p-channel lateral SiGe-on-insulator tunnel FET with increase in Ge content, x ($L = 100$ nm, $t_{ox} = 2$ nm, p-polysilicon gate).*

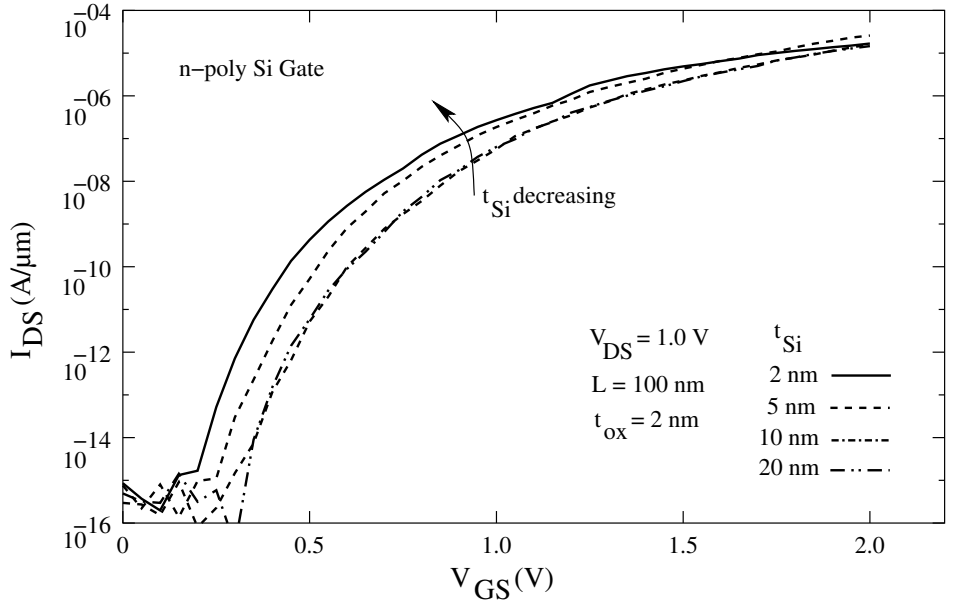

Figure 6.4: *Transfer characteristics for a lateral SOI tunnel FET with change in silicon layer thickness ($L = 100$ nm, $t_{ox} = 2$ nm, $x = 0.0$, n-polysilicon gate).*

Chapter 7

Conclusions and Future Work

In this thesis, a basic understanding of the working of the tunnel FETs has been developed by means of 2-D computer device simulations. The validity of the models used has been verified by experimental results, and the electrical parameters have been accordingly redefined for the tunnel FETs. In addition to this, a novel way of improving the device performance by use of SiGe has been proposed. It is further shown that using SiGe and gate workfunction engineering, the tunnel FETs can be scaled maintaing large on/off current ratios. This is because the effective sub-threshold swing of tunnel FETs can be scaled to below the 60 mV/dec limit of conventional MOSFETs. Since having pseudomorphically strained SiGe delta layer results in asymmetry in the n-channel as well as the p-channel performance, Finally, a new lateral tunnel FET with pseudomorphically strained SiGe layer to further enhance the tunnel FET performance is proposed. Thus, the device shows a lot of promise for future scaled CMOS technologies, for both high-speed as well as low-operating power applications, for digital as well as analog applications.

In chapter 5 experimental verification of some of the properties of the tunnel FETs is given. However, there is much more remains to be done. One of them is the experimental realization of the SiGe devices and experimental verification of the sub-60 mV/dec swing that can be achieved even for the silicon tunnel FETs. This has not yet been demonstrated in literature. Further, as it has been theoretically shown here, the possiblity of optimzing the silicon homogeneous tunnel FETs to achieve a sub-60 mV/dec room temperature swing should be explored.

For the case of lateral symmetric n-channel and p-channel tunnel FET as proposed in Chapter 6, a detailed investigation of the device is needed so as to optimize it for improved performance. As with SiGe channel, stable thermal oxide cannot be grown, there is need to optimize the existing technology to incorporate high-κ gate materials. Further, to improve the doping profile, it is essential to optimize the fabrication of the devices at lower temperatures. In order to have a symmetric performance and low off-currents for scaled tunnel FETs, gate electrode materials, other than n-polysilicon and p-polysilicon will be needed. As workfunction tunable metals as gate electrodes have already been proposed in literature, these should be investigated for the tunnel FETs.

Appendix A

Electric Field and Potential for Tunnel FET Junctions

p-π-n junction

Poisson's equations are solved here in order to derive a general solution for potential, (ψ), and electric field, E, in a p-π-n diode. The doping in the three regions is N_N (n-type), N_i (n-type, $N_i << N_N$) and N_A (p-type) in the n, π and p regions respectively. The depletion region across the junction is divided into three parts, as shown in Fig. A.1.

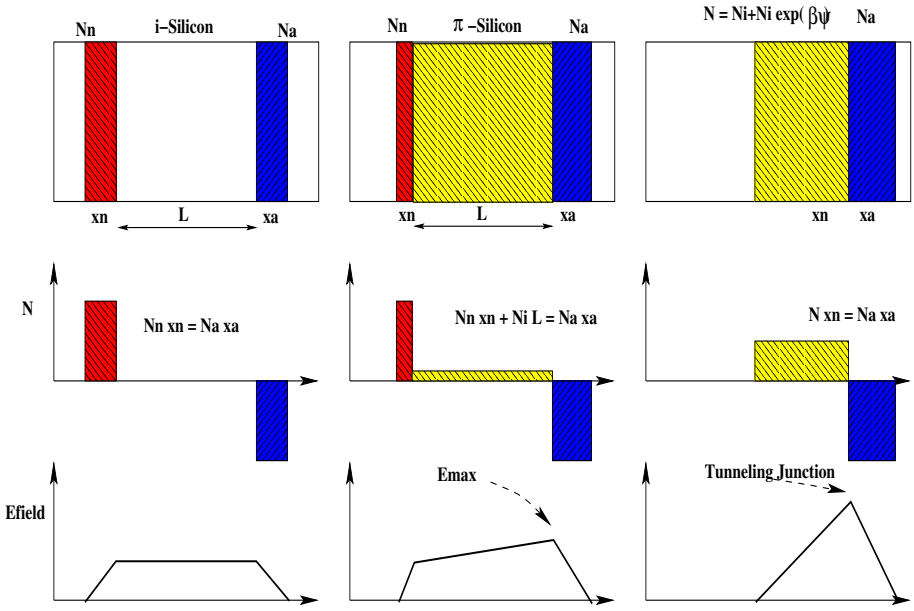

Figure A.1: *Schematic representation of E and ψ for a p-i-n, p-π-n and a p-n junction*

1. In the n^+ region extending from $x = -x_n$ to $x = 0$,
2. In the n^- channel region from $x = 0$ to $x = L$, and
3. In the p^+ region extending from $x = L$ to $x = x_a$.

The Equations

Defining the potential in the three regions as, $\psi_1(x)$, $\psi_2(x)$ and $\psi_3(x)$ and correspondingly, the electric fields as, $E_1(x)$, $E_2(x)$, $E_3(x)$, the Poisson's equations in the three regions can be written as,

$$\nabla^2\psi_1(x) = -qN_N/\epsilon_s, (-x_n \leq x \leq 0) \quad \text{(A.1)}$$
$$\nabla^2\psi_2(x) = -qN_i/\epsilon_s, (0 \leq x \leq L) \quad \text{(A.2)}$$
$$\nabla^2\psi_3(x) = qN_A/\epsilon_s, (L \leq x \leq x_a) \quad \text{(A.3)}$$

Boundary Conditions

The boundary conditions for the p-π-n diode are,

$$\psi_2(L) = \psi_3(L) \quad \text{(A.4)}$$
$$\psi_1(0) = \psi_2(0) \quad \text{(A.5)}$$
$$\psi_1(-x_n) = \psi_0 \quad \text{(A.6)}$$
$$\psi_3(L + x_a) = 0 \quad \text{(A.7)}$$
$$E_1(-x_n) = 0 \quad \text{(A.8)}$$
$$E_1(0) = E_2(0) \quad \text{(A.9)}$$
$$E_3(L + x_a) = 0 \quad \text{(A.10)}$$
$$E_2(L) = E_3(L) \quad \text{(A.11)}$$

Solution

Solving Eq. A.1-A.3, for boundary conditions A.5-A.10, we get the following expressions for E and ψ in the three depletion regions.

$$E_1(x) = \frac{qN_N}{\epsilon_s}(x + x_n) \quad \text{(A.12)}$$
$$E_2(x) = \frac{q}{\epsilon_s}(N_i x + N_N x_n) \quad \text{(A.13)}$$
$$E_3(x) = \frac{qN_A}{\epsilon_s}(x - L - x_a) \quad \text{(A.14)}$$
$$\psi_1(x) = -\frac{qN_N}{2\epsilon_s}(x + x_n)^2 + \psi_0 \quad \text{(A.15)}$$
$$\psi_2(x) = -\frac{q}{2\epsilon_s}(N_i x^2 + 2N_N x_n x + N_N x_n^2) + \psi_0 \quad \text{(A.16)}$$
$$\psi_3(x) = \frac{qN_A}{2\epsilon_s}(x - L - x_a)^2 \quad \text{(A.17)}$$

From boundary conditions A.4, we get the charge neutrality condition,

$$x_n N_N + N_i L = N_A x_a \quad \text{(A.18)}$$

and A.11, we get,

$$N_N x_n^2 + (2N_N L)x_n + (N_i L^2 + N_A x_a^2 - \frac{2\epsilon_s}{q}\psi_0) = 0 \tag{A.19}$$

Simplifying for the case $N_A = N = N_N$ and using the built-in potential,

$$\psi_0 = \frac{kT}{q} log \frac{N_N N_A}{n_i n_i}$$

we get for x_n and x_a,

$$x_n = \frac{1}{2L(1 - N_i/N)}[\frac{2\psi_0\epsilon_s}{qN} - \frac{L^2 N_i}{N} + \frac{N_i^2 L^2}{N^2}] \tag{A.20}$$

$$x_a = x_n + \frac{N_i L}{N} \tag{A.21}$$

Thus, the maximum electric field at the π-p junction (the tunneling junction of a n-channel tunnel FET), $E_{max-p\pi n} = E_2(L) = E_3(L)$, then can be written as from equations A.13 and A.14,

$$E_{max-p\pi n} = \frac{q}{\epsilon_s}(N_i L + N x_n) \tag{A.22}$$

where x_n is given from Eq. A.20.

p-i-n junction

Simplifying the above equations for $N_i << N$, the case of a p-i-n junction, we get from Eq. A.20 and A.21,

$$x_n \approx \frac{\psi_0\epsilon_s}{qNL} \tag{A.23}$$

$$x_a \approx x_n \tag{A.24}$$

Thus, the maximum electric field at the i-p junction (the case when tunnel FET is 'off' at $V_{GS} = 0$ V), $E_{max} = E_2(L) = E_3(L)$, from equations A.13, A.14 and A.22, can be written as,

$$E_{max-pin} = \frac{qN}{\epsilon_s} x_a \tag{A.25}$$

$$\approx \frac{\psi_0}{L} \tag{A.26}$$

p-π-n junction with varying N_i

A very simple case is considered here to study the effect of surface potential on the p-π-n junction E_{max} and ψ. Assuming the charge in the channel (π region) to be uniform (N_i), and on application of a surface potential, ψ_s, the total electron concentration increasing as,

$$N_\pi = N_i + N_i exp(\frac{q}{kT}\psi_s) \tag{A.27}$$

The $E_{max-p\pi n}$ equations A.22 and A.20 for $E_{max-p\pi n}$ and x_n respectively, become,

$$E_{max-p\pi n} = \frac{q}{\epsilon_s}(N_\pi L + N x_n) \tag{A.28}$$

$$x_n = \frac{1}{2L(1-N_\pi/N)}[\frac{2\psi_0\epsilon_s}{qN} - \frac{L^2 N_\pi}{N} + \frac{N_\pi^2 L^2}{N^2}] \tag{A.29}$$

$$x_a = x_n + \frac{N_\pi L}{N} \tag{A.30}$$

p-n junction with varying doping in n-region

When a positive gate potential is applied to the tunnel FET, a n-p tunnel junction is formed between the n^- channel and the p source. Applying a similar approach as in the above sections, and solving for a n-p junction with charge in the n region given by N_π, we get the maximum electric field at the tunneling junction, E_{max-pn} as,

$$E_{max-pn} = \sqrt{\frac{2q\psi_0 N_A}{\epsilon_s}}\{1 + \frac{N_i}{N_A} exp(-\frac{q}{kT}\psi_s)\}^{-1/2} \tag{A.31}$$

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MEDICI Constants

1. Substrate orientation = < 100 >
2. k = 8.61738 $\times 10^{-05}$ eV/K
3. q = 1.60218 $\times 10^{-19}$ C
4. ϵ_0 = 8.85418 $\times 10^{-14}$ F/cm
5. T = 300.0 K
6. $V_t(kT/q)$ = 0.025852 V
7. n_i(T) = 1.4473 $\times 10^{10}$ (cm^{-3})
8. v_{satn} (T) = 1.0349 $\times 10^{7}$ (cm/sec)
9. v_{satp} (T) = 1.0349 $\times 10^{7}$ (cm/sec)
10. E_g (T) = 1.0800 (eV)
11. A_{kane} = 3.5$\times 10^{21}$ (eV$^{1/2}$/cm-s-V^2)
12. B_{kane} = 22.5$\times 10^{6}$ (V/cm-eV$^{3/2}$)
13. N_c (T) = 2.8000 $\times 10^{19}$ (cm^{-3})
14. N_v (T) = 1.0400 $\times 10^{19}$ (cm^{-3})
15. v_{surfn} (T) = 2.2068 $\times 10^{6}$ (cm/sec)
16. v_{surfp} (T) = 1.6204 $\times 10^{6}$ (cm/sec)

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Directly related to this work

1. S. Sedlmaier, **K. K. Bhuwalka**, A. Ludsteck, C. Tolskdorf, J. Schulze, W. Hansch, and I. Eisele, "MBE grown vertical tunnel FET for low-power circuits," *12^{th} Euro-MBE Workshop*, Congress Center, Bad Hofgastein, Austria, 2003.

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4. **Krishna K Bhuwalka**, Jörg Schulze, Ignaz Eisele, "Scaling issues of n-channel vertical tunnel FET with δp$^+$ SiGe layer," *62^{nd} Device Research Conference Digest*, Notre Dame, Indiana, USA, vol. 1, pp. 215-216, 21-23 June 2004.

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Invited Talks

27. **Krishna K. Bhuwalka**, J. Schulze, I. Eisele, "Vertical tunnel field-effect transistors," Department of Electrical Engineering, University of California Riverside, CA, USA, June 28, 2004.

28. **Krishna K Bhuwalka**, M. Born, I. Eisele, "Sub-60 mV/dec effective subthreshold swing tunnel transistors for CMOS applications," Swiss Federal Institute of Technology Lausanne (EPFL), Switzerland, July 1, 2005.

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Curriculum Vitae

Krishna Kumar Bhuwalka, was born on the 27^{th} April 1976 in Asansol, India, to Shyam Sunder Bhuwalka and Nirmala Devi. He is a citizen of The Republic of India. He recieved the B.Sc degree in Physics from Hindu College, University of Delhi in 1998; the M.Sc degree in Physics from the Indian Institute of Technology (IIT) Kanpur in 2000; and the M.Tech degree in Microelectronics from IIT Bombay in 2002. From May to July 1999 he was with the Department of Astronomy and Astrophysics, Tata Institute of Fundamental Research (TIFR), Mumbai studying characteristics of proportional counters for X-ray astronomy; and from June to July 2004 he was with the Department of Electrical Engineering, University of California Riverside, USA, where he investigated 1-D quantum mechanical effects with delta doped Si/SiGe layers in tunnel FETs. He is currently a post-doctoral researcher at Institute of Physics, Faculty of Electrical and Information Technology, Universitaet der Bundeswehr, Munich.

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"To the electron-

may it never be of any use to anybody."

favourite toast at annual dinners at
Cavendish Laboratory, early 1900's.